SENSE

Enhancing Microarchitectural Awareness for TEEs via Subscription-Based Notification

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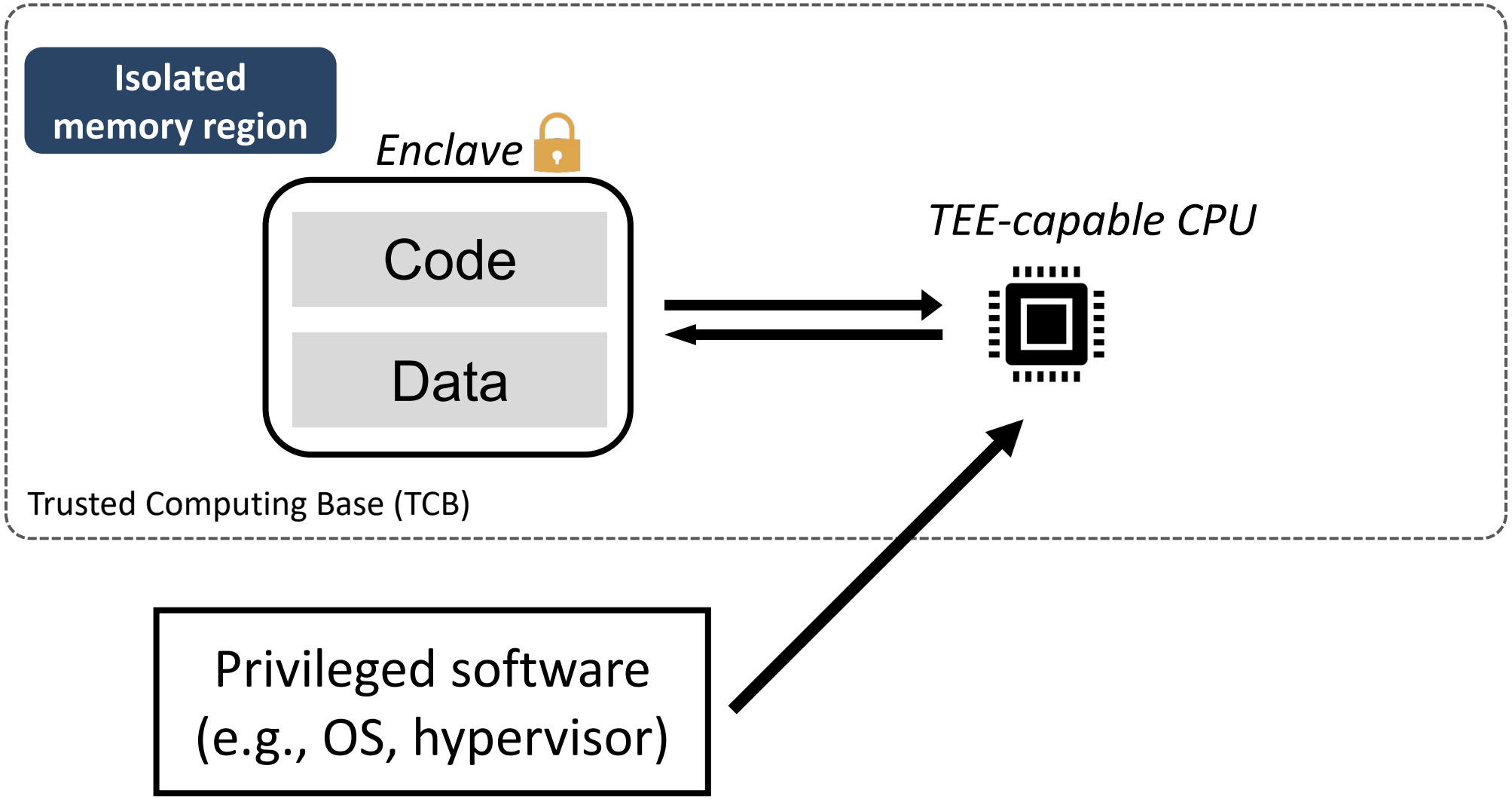
Scott Constable[2], Yuan Xiao[2], Michael Steiner[2], Mona Vij[2], Taesoo Kim[1]

[1]Georgia Institute of Technology, [2]Intel, [3]George Mason University, [4]University of Waterloo

TEE 101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Privileged software (e.g., OS, hypervisor)

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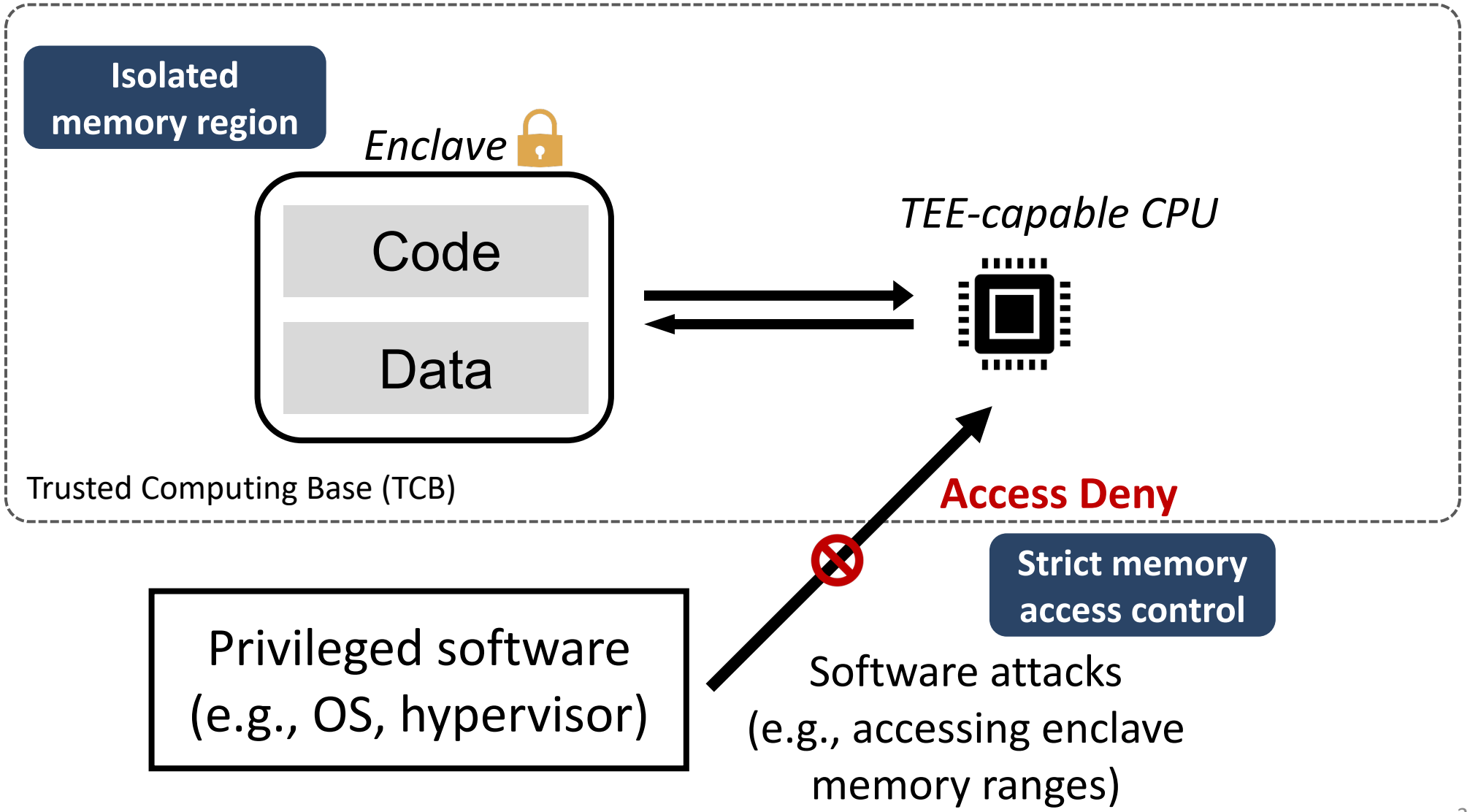
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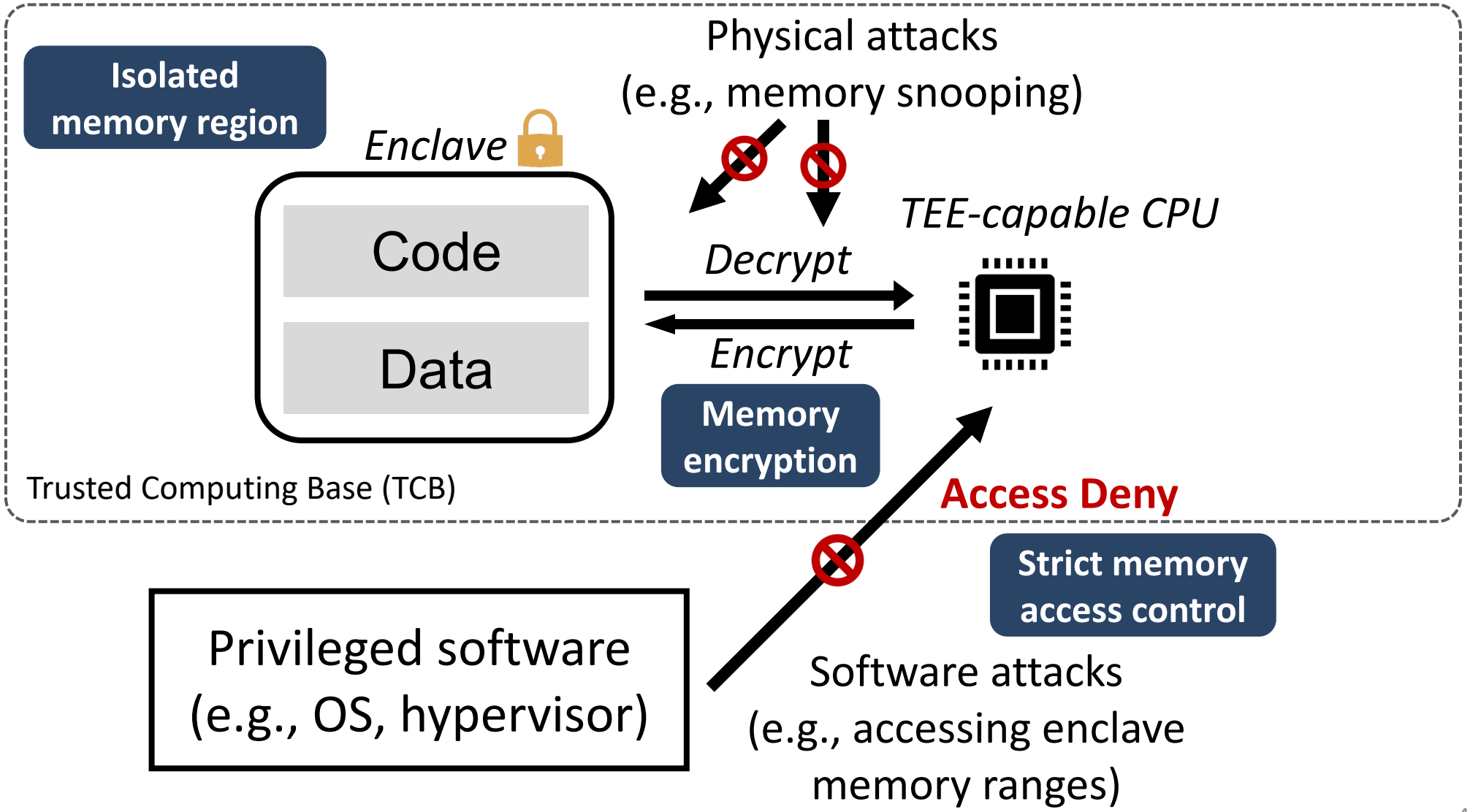
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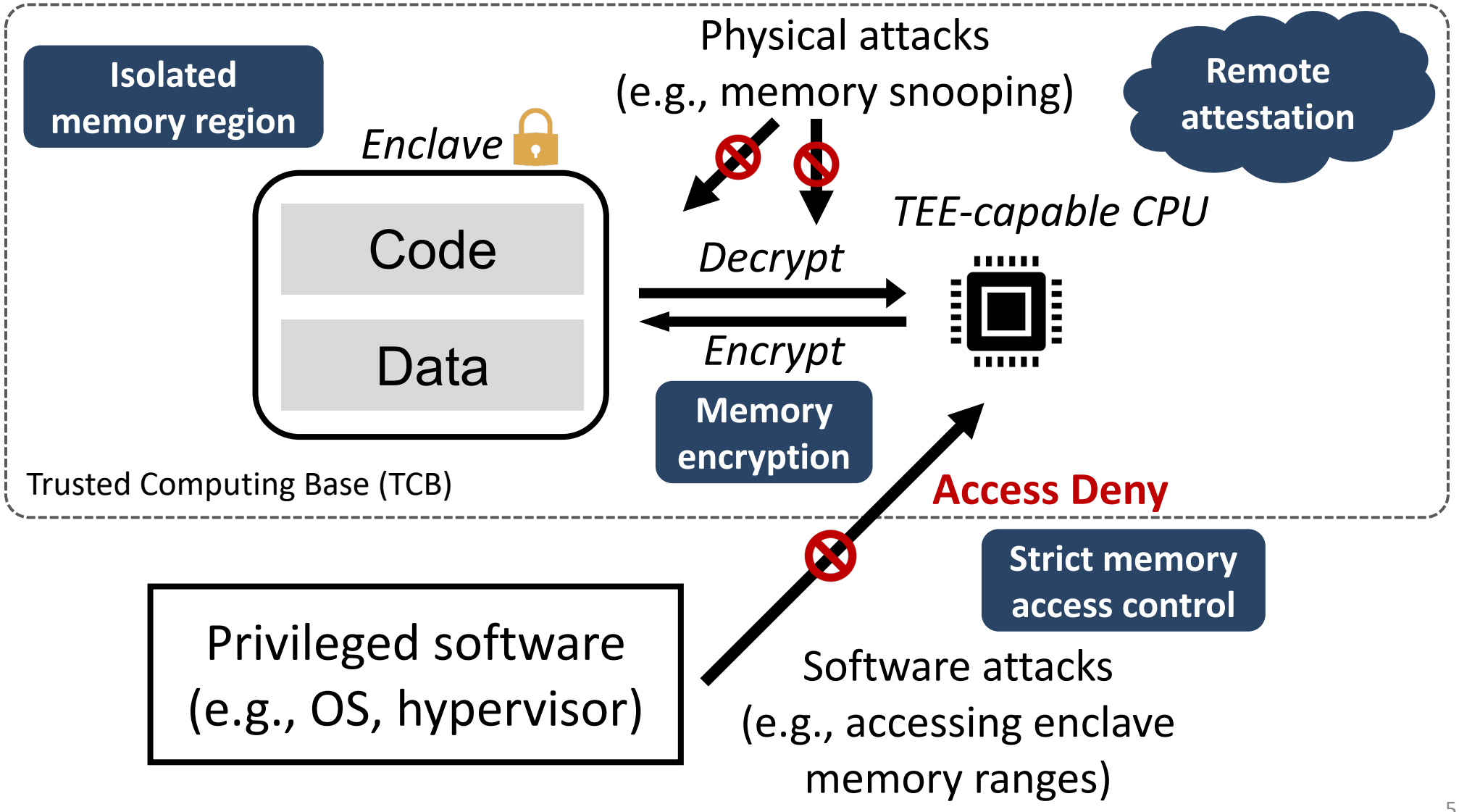
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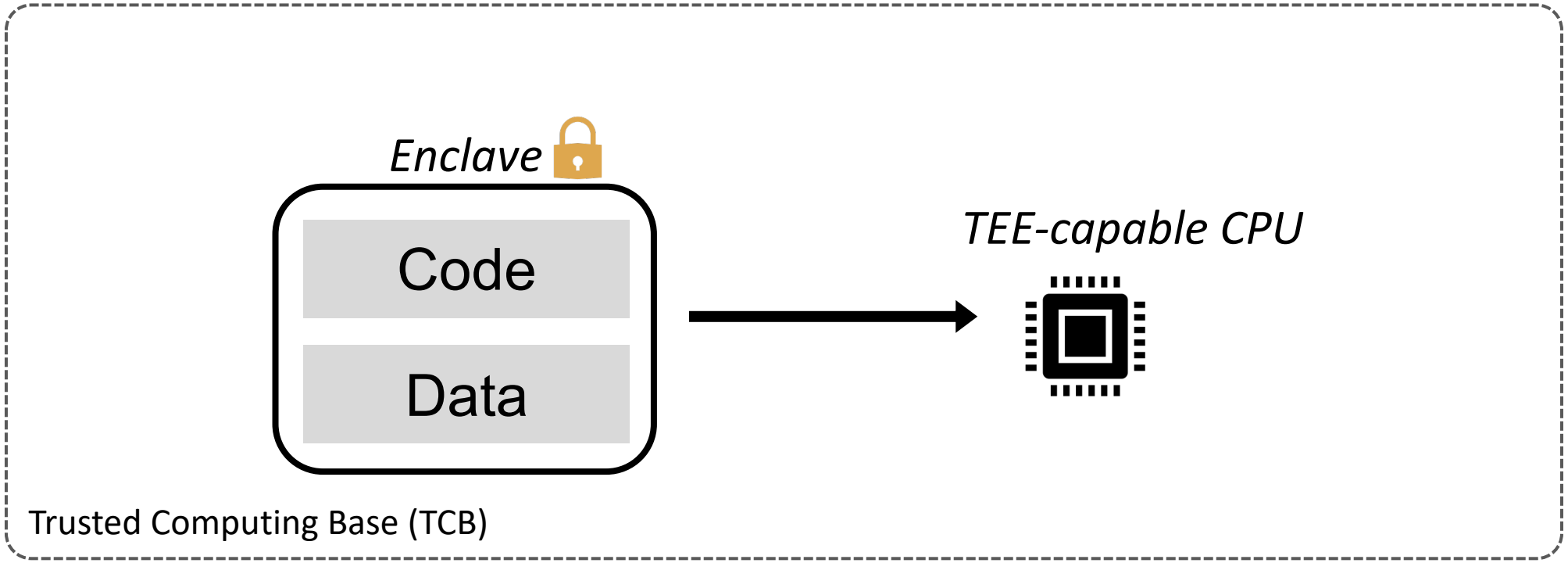
Achilles' Heel: Side-Channel Attacks (SCAs)



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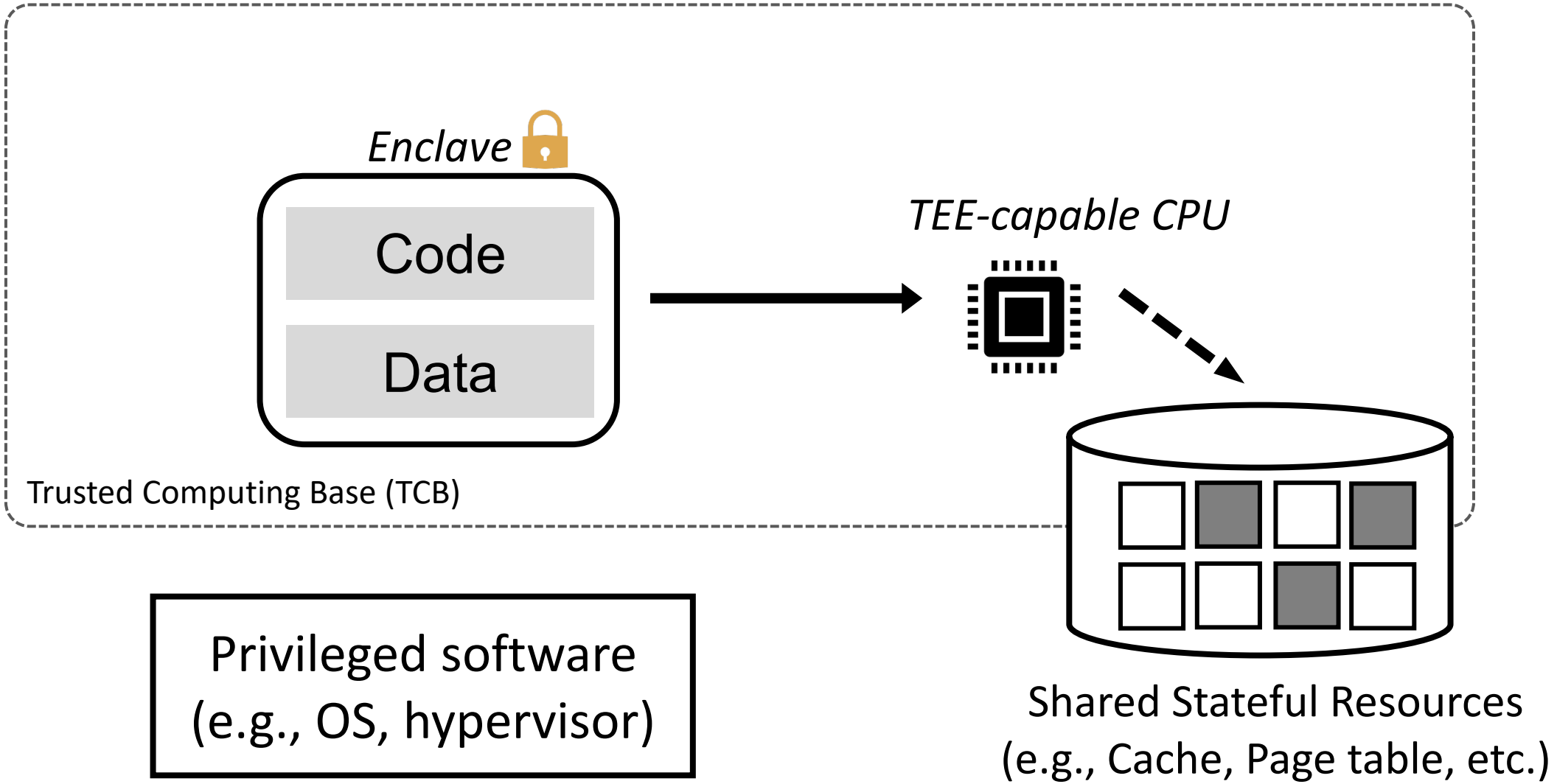

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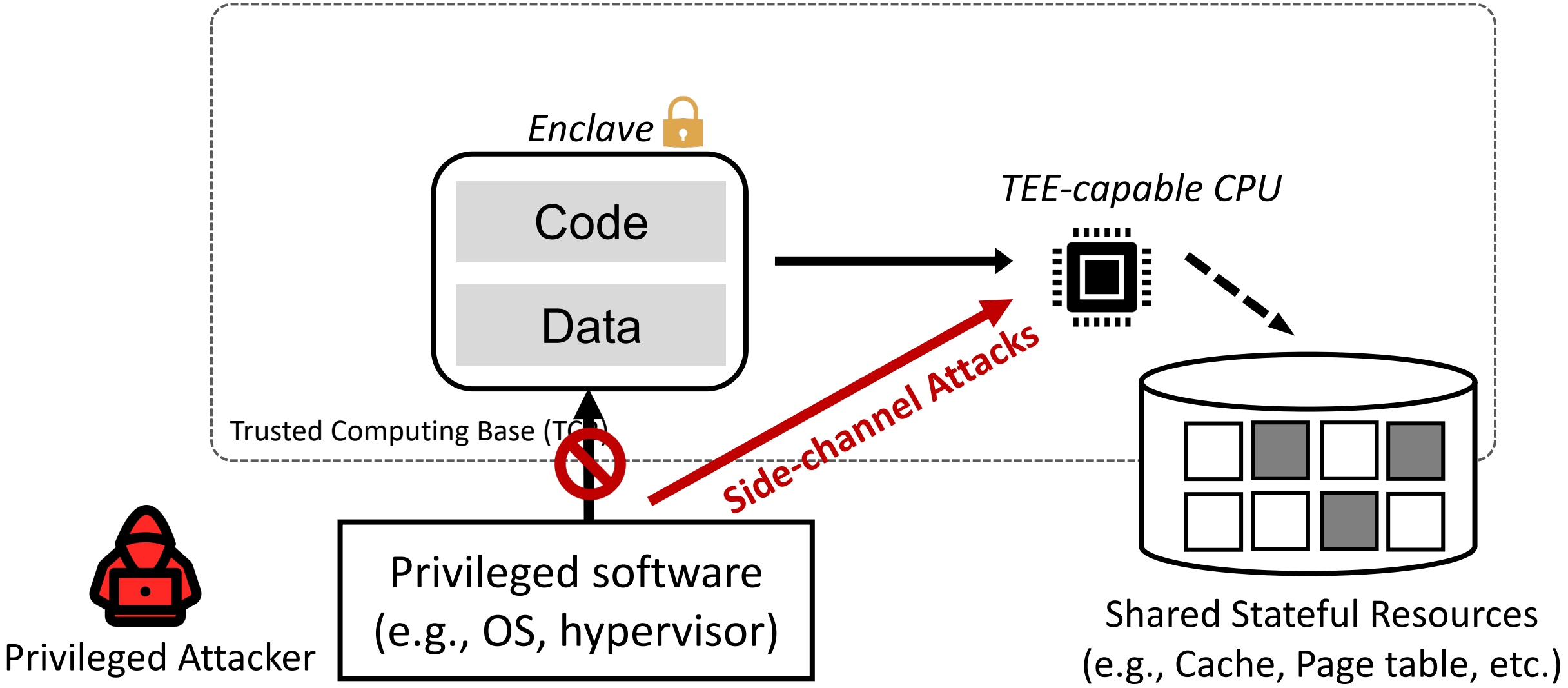

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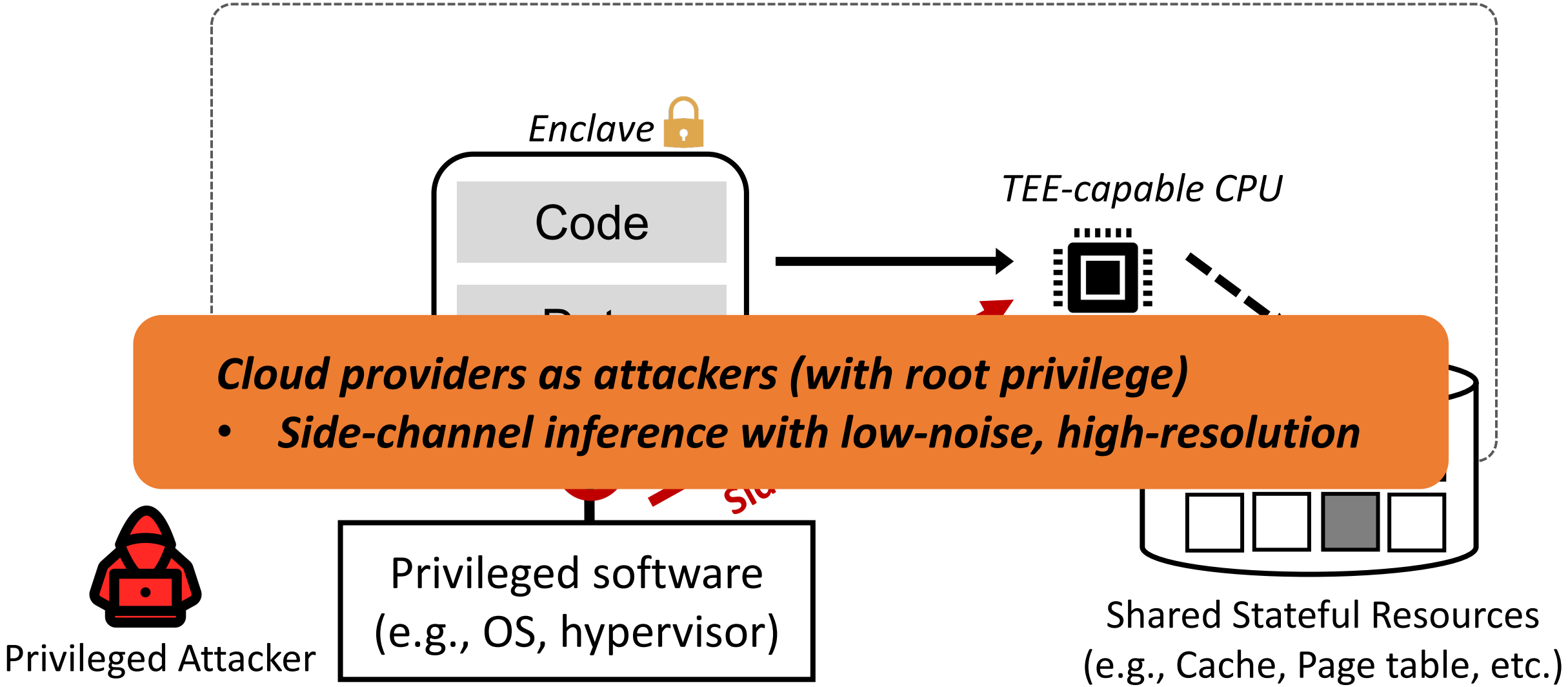

Existing Defenses

- Hardware resource isolation
  - \+ Robust defense that mitigates the root causes of leakage
  - − Software cannot benefit from resource sharing

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  - − Software cannot benefit from resource sharing
- Detection-based defenses
  - + Permits resource sharing
  - − Leaks at a lower rate, or lacks flexibility

Detection Defenses: Performance Counters

- Assumption: SCAs have impact on victim's performance
  - Detect SCAs by observing such performance characteristics [1-3]
  - Rely on OS interface to collect microarchitectural information
- Limitations:
  - Coarse-grained statistical data
  - Limited victim responses

[1] M. Chiappetta, E. Savas, and C. Yilmaz, "Real time detection of cache-based side-channel attacks using hardware performance counters," Applied Soft Computing, vol. 49, pp. 1162–1174, 2016.

[2] J. Chen and G. Venkataramani, "Cc-hunter: Uncovering covert timing channels on shared processor hardware," in Proceedings of the 47th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO), Cambridge, UK, Dec. 2014.

[3] Replayconfusion: Detecting cache-based covert channel attacks using record and replay," in Proceedings of the 49th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO), Taipei, Taiwan, Oct. 2016.

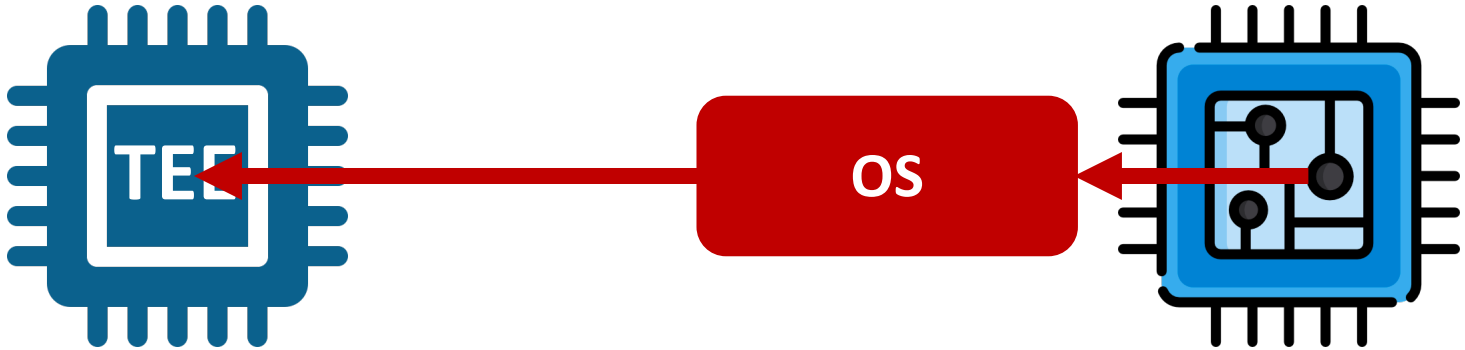
Detection Defenses: HTM

- Hardware Transactional Memory (HTM) provides safe concurrency
- Cloak [4] uses Intel® Transactional Synchronization Extensions (Intel® TSX, an HTM implementation) to mitigate cache side channels

[4] D. Gruss, J. Lettner, F. Schuster, O. Ohrimenko, I. Haller, and M. Costa, “Strong and Efficient Cache Side-Channel Protection using Hardware Transactional Memory,” in Proceedings of the 26th USENIX Security Symposium (Security), Vancouver, Canada, Aug. 2017.

Detection-Based Defenses under TEE

- Missing trusted data sources in TEEs



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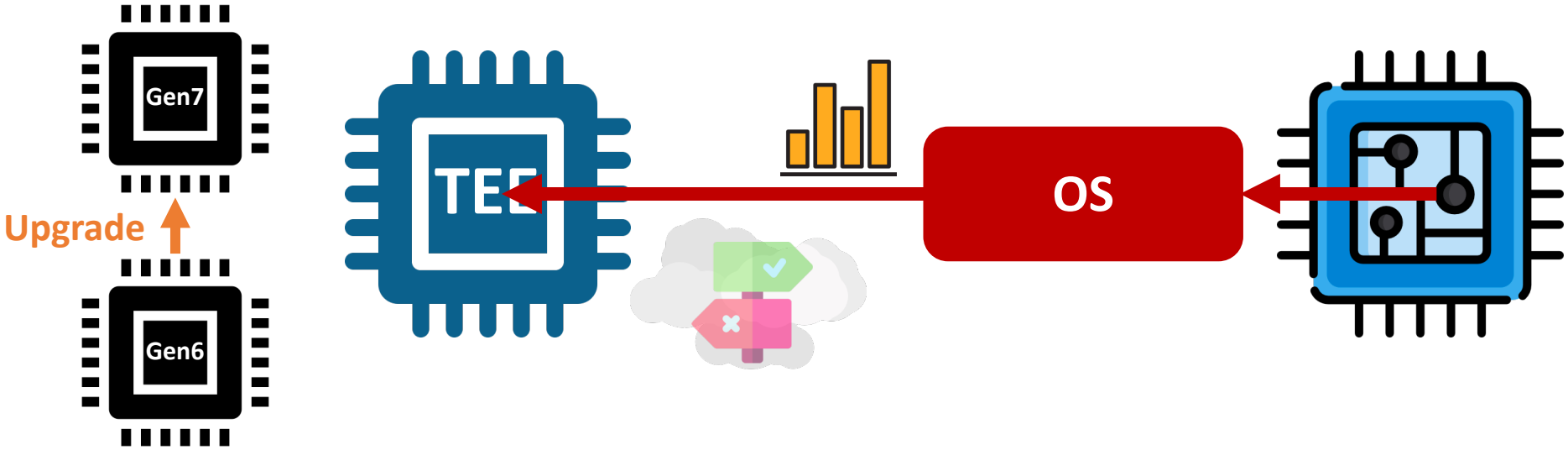

An Irony – Information Asymmetry

- TEE as a security container is constraining victims' ability to reliably gather SCA signals
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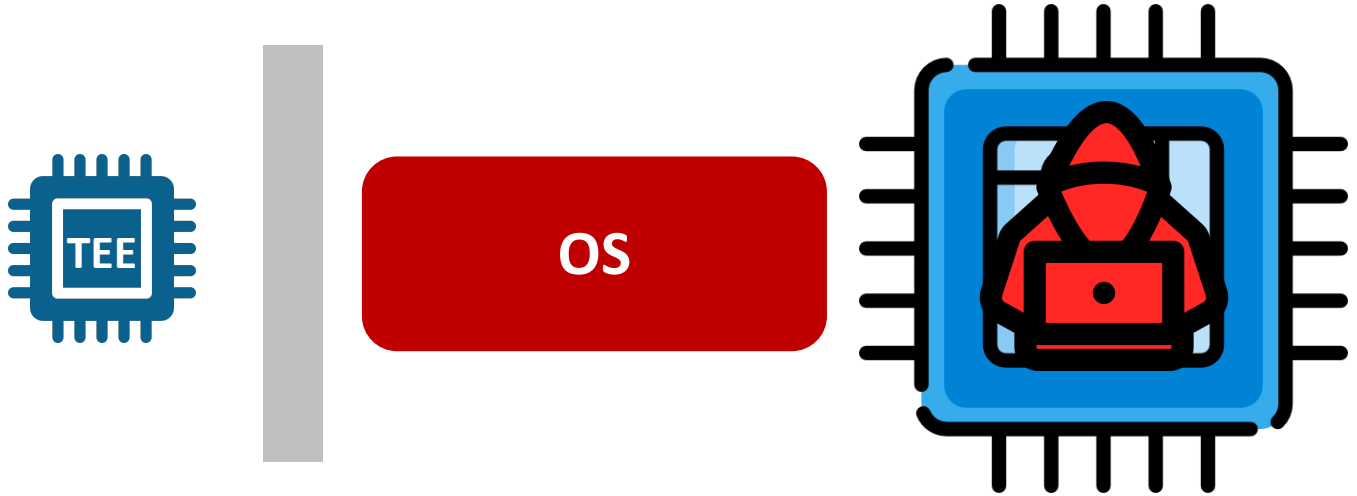

The victim always sits at a disadvantaged position

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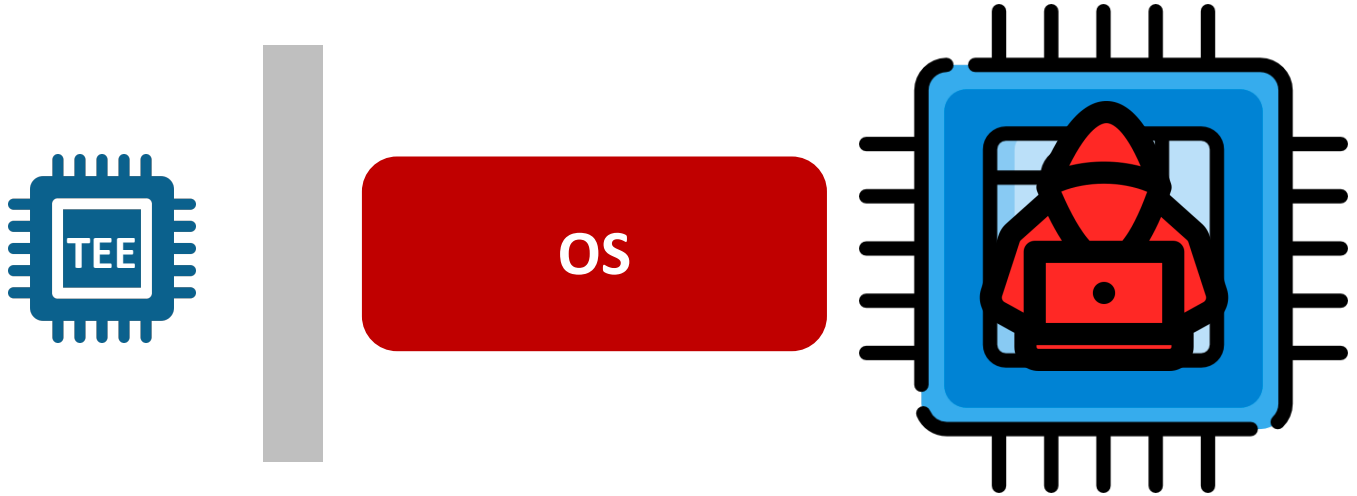

Can we make detection-based defenses more robust?

Goals of SENSE

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- Extensibility
  - Ready for new events in the future

Overview of SENSE

- An architectural extension that directly exposes microarchitectural events to userspace TEEs, using three steps:

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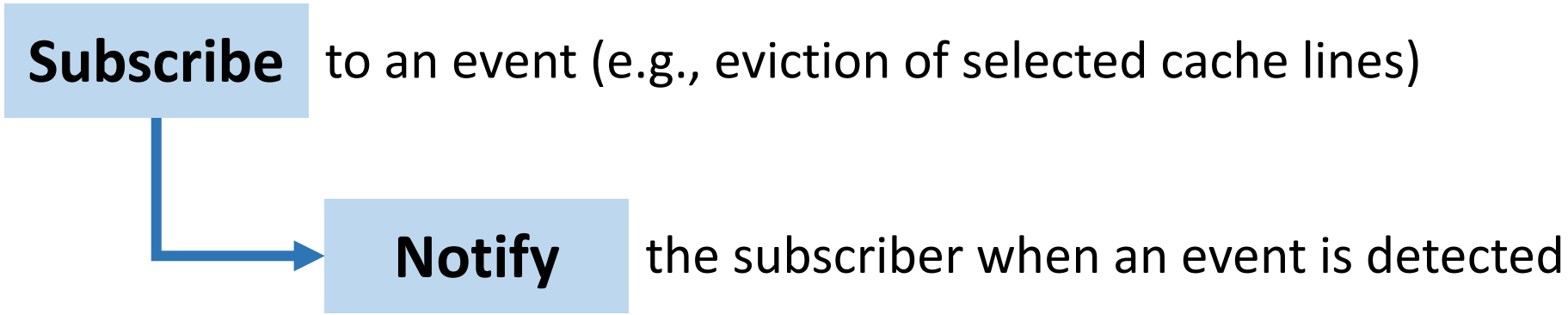

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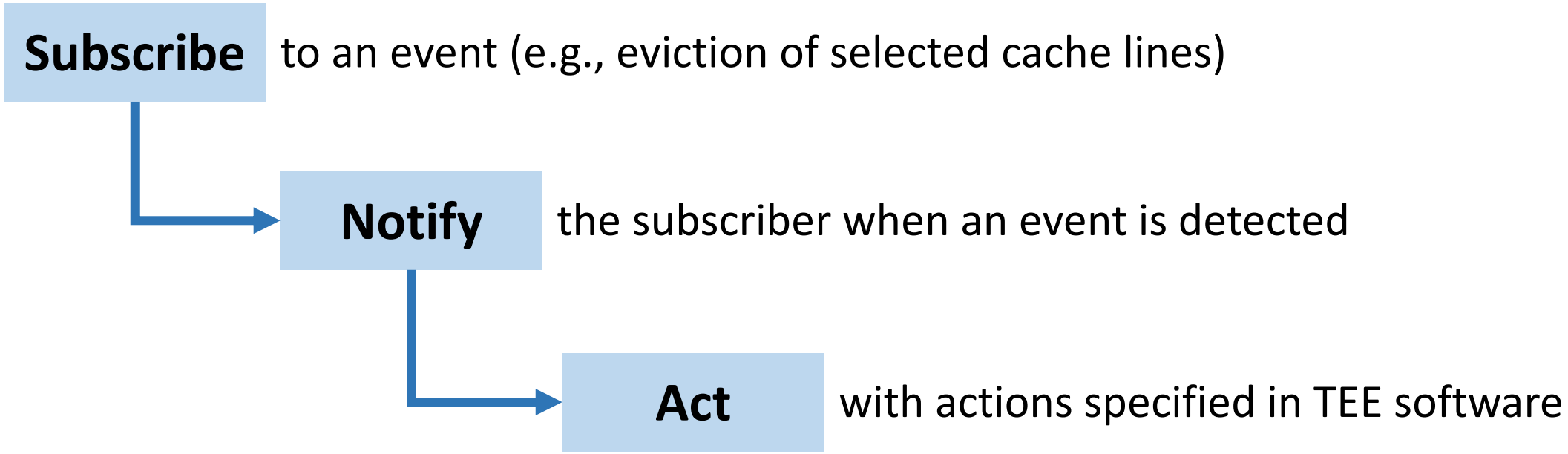
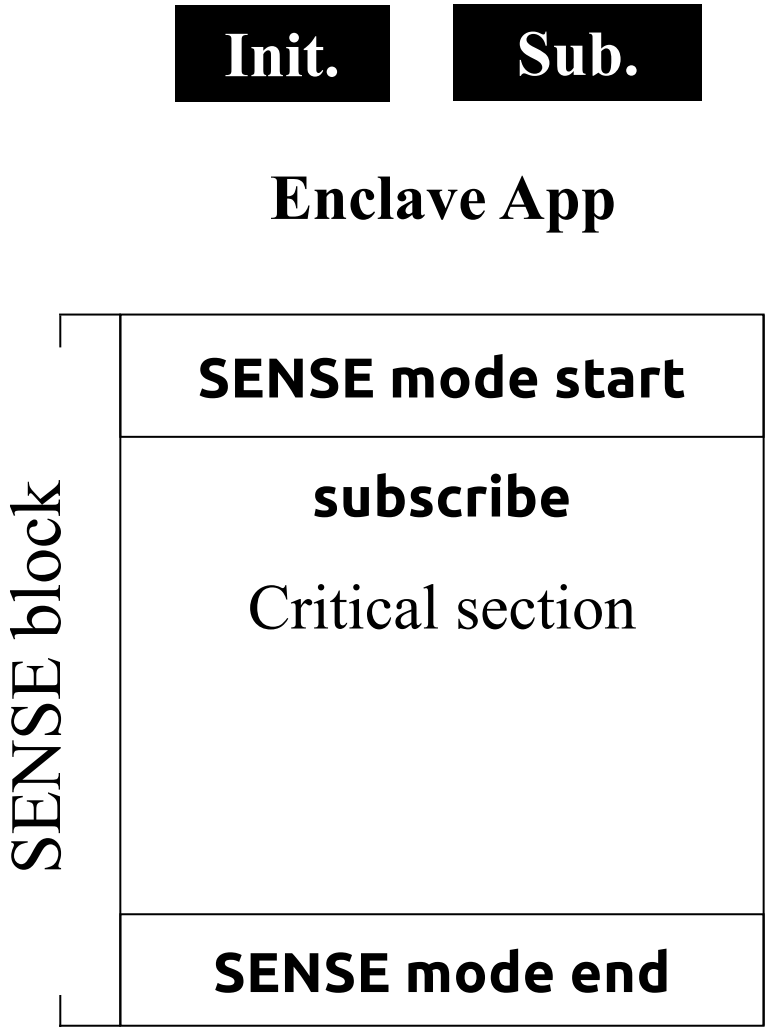


SENSE in Action



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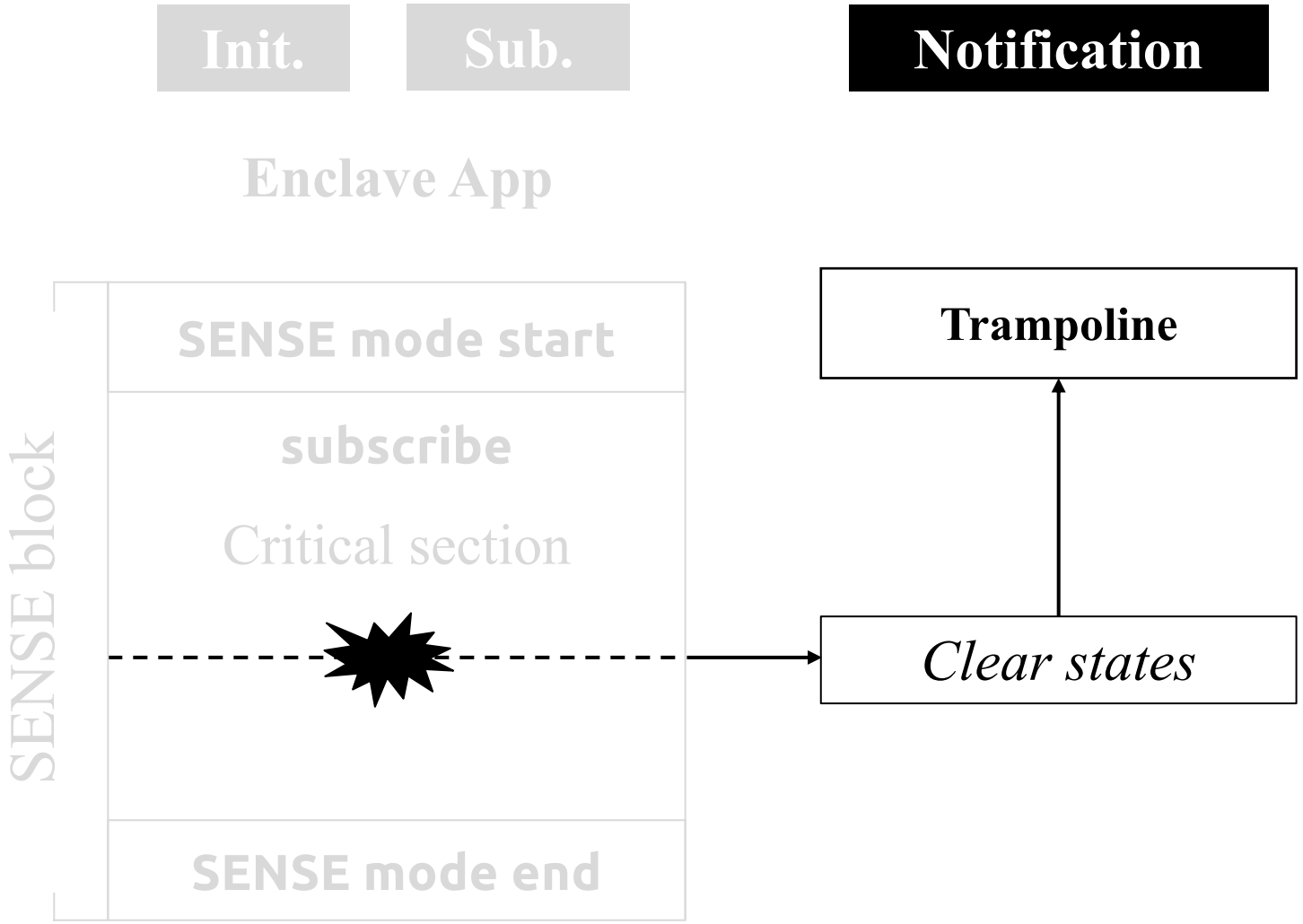

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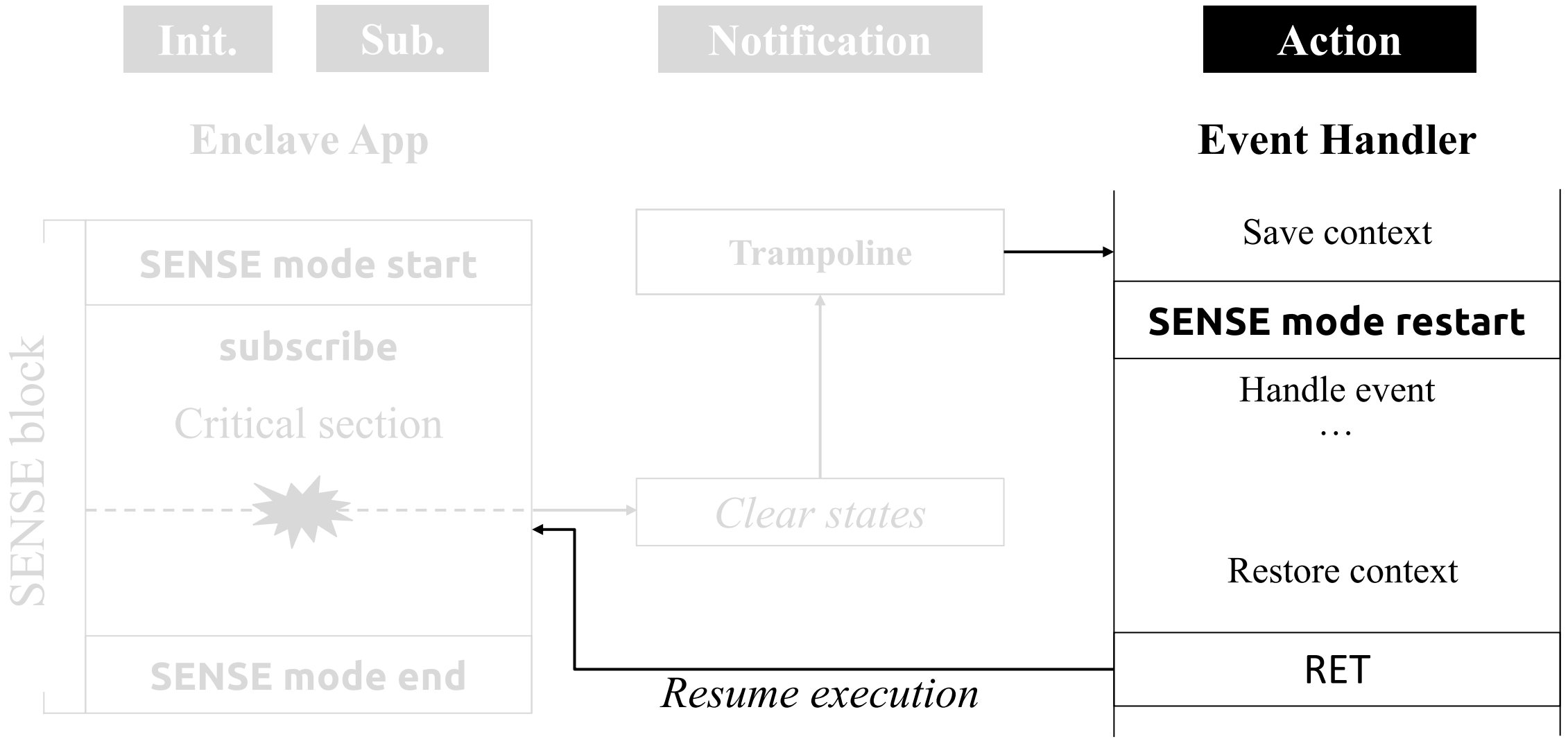

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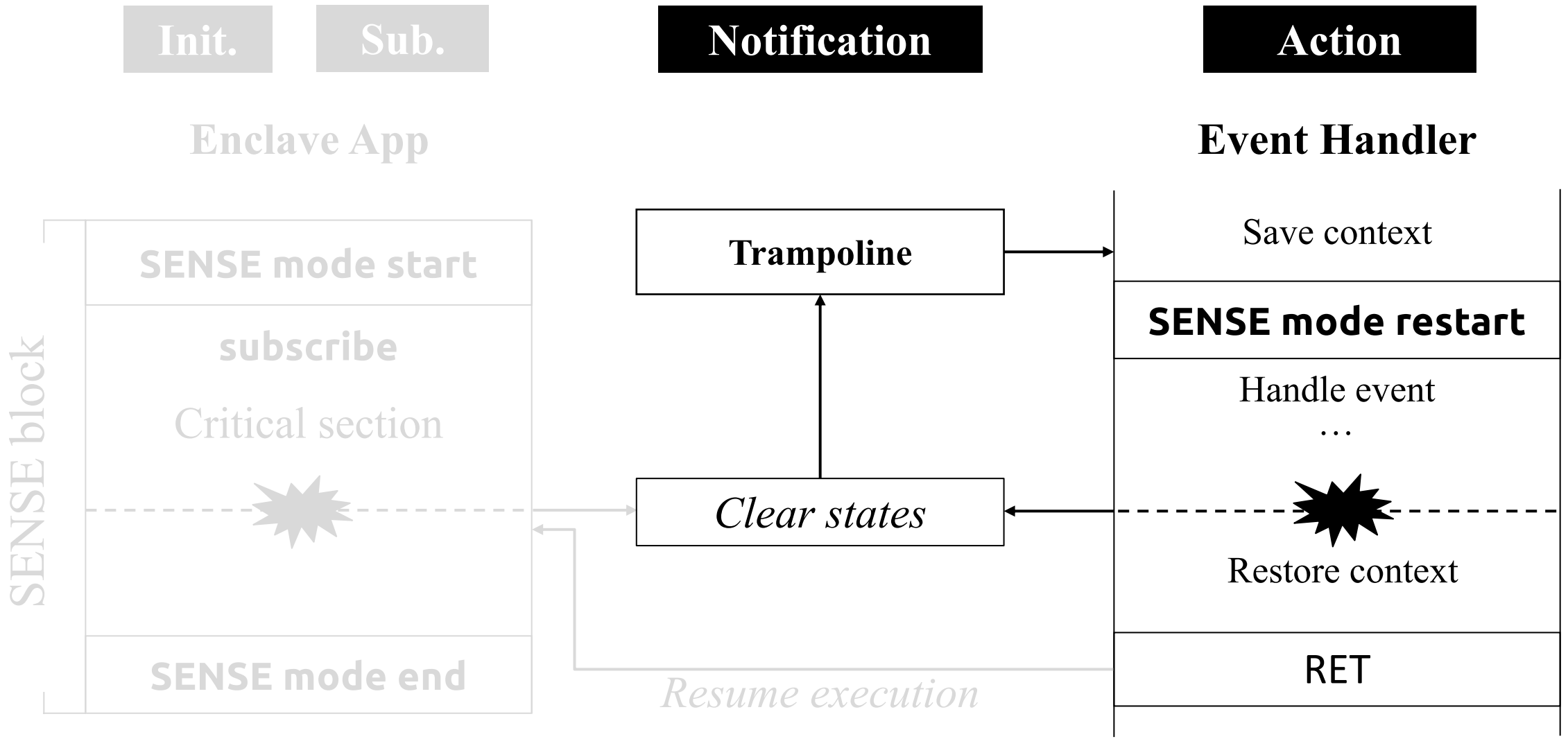

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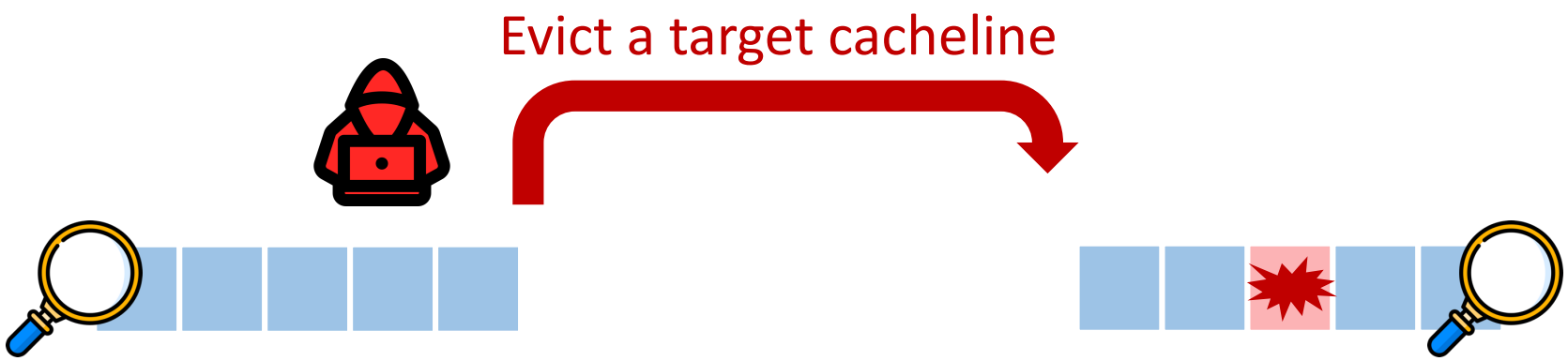

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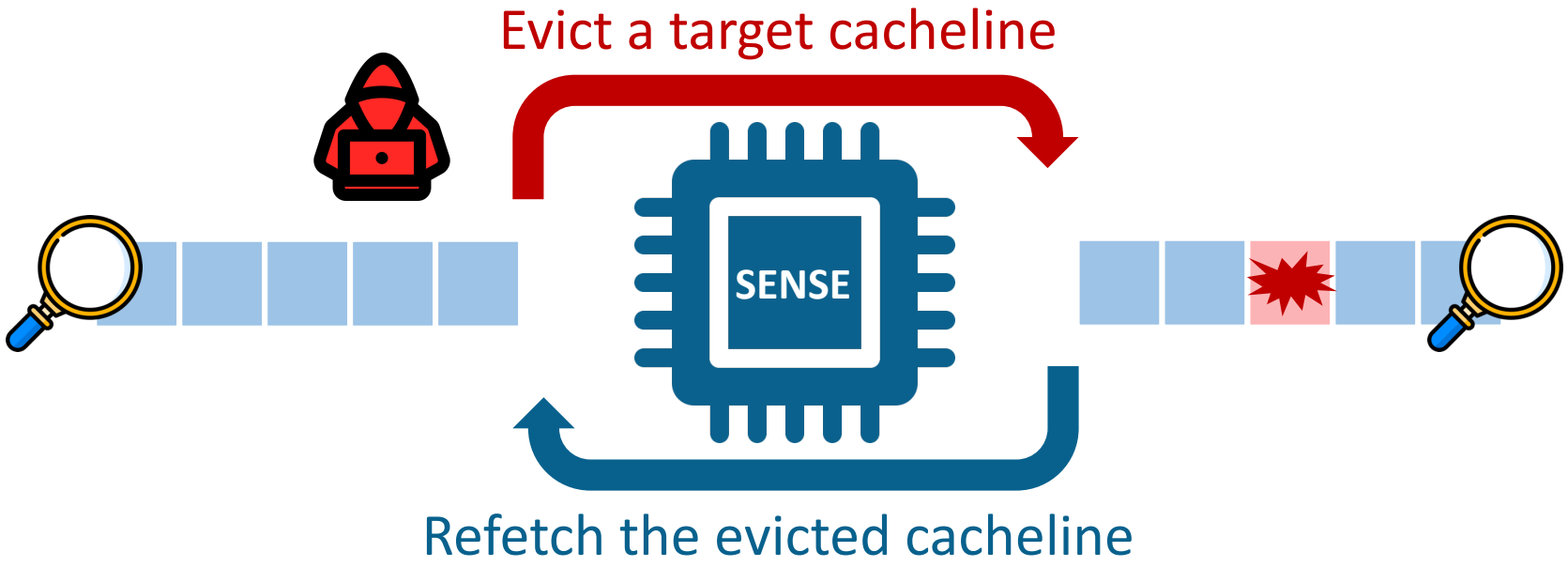
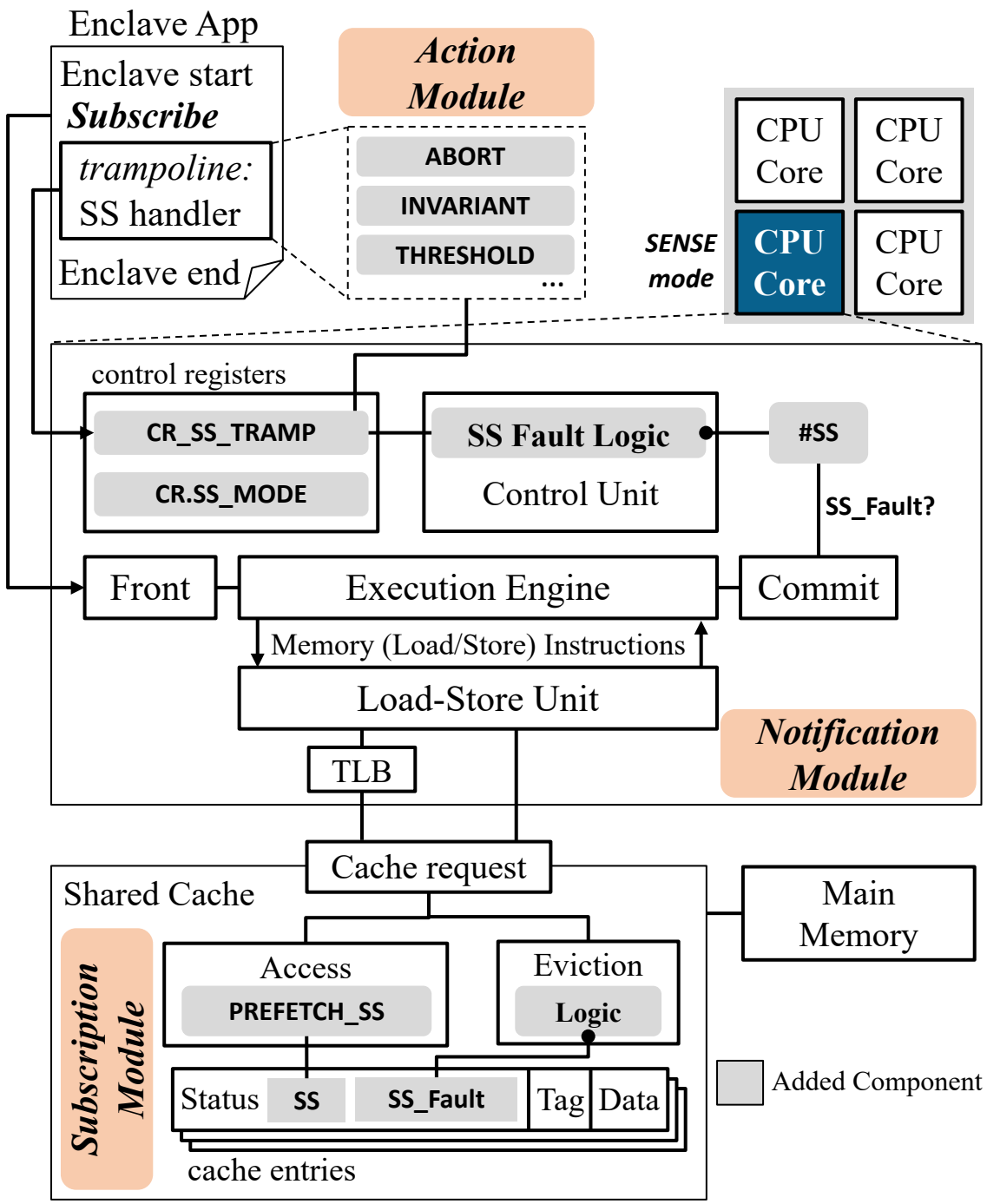
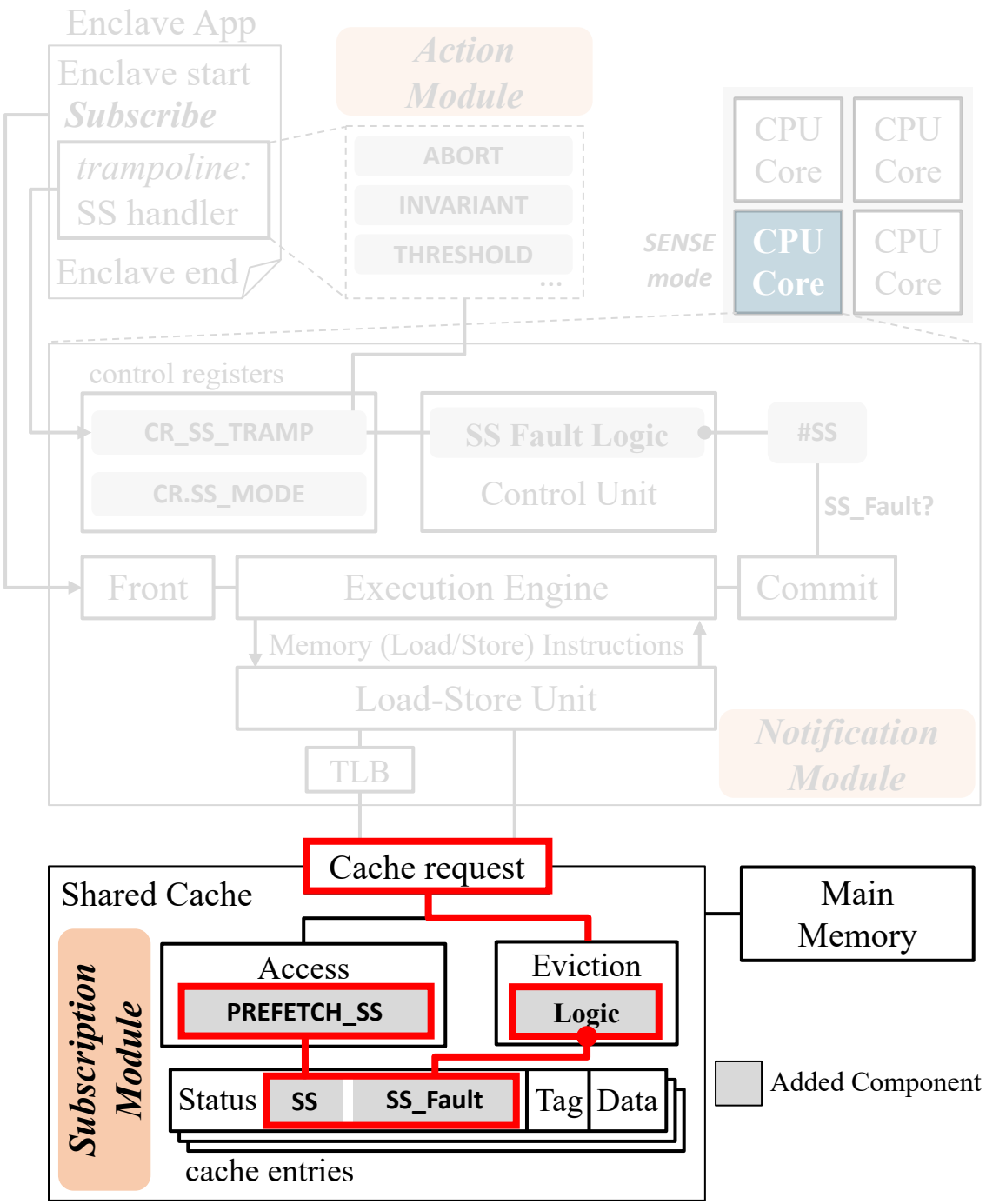


Architecture



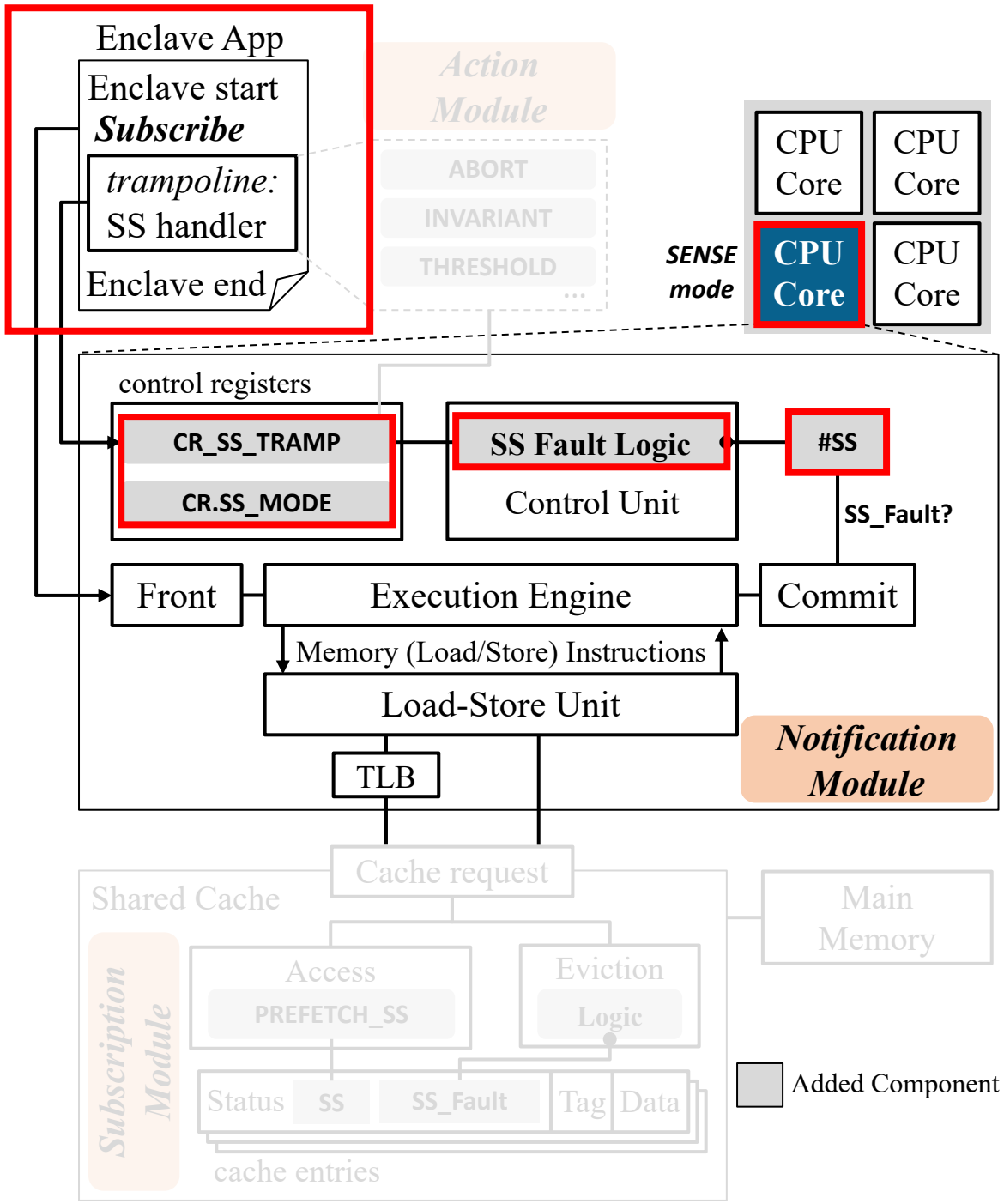
Subscription Module

- Subscription request as a specialized memory request
- SENSE status bits in each cache entry for status monitoring
- Check the monitoring status during eviction
- Inform the notification module in the cache request response



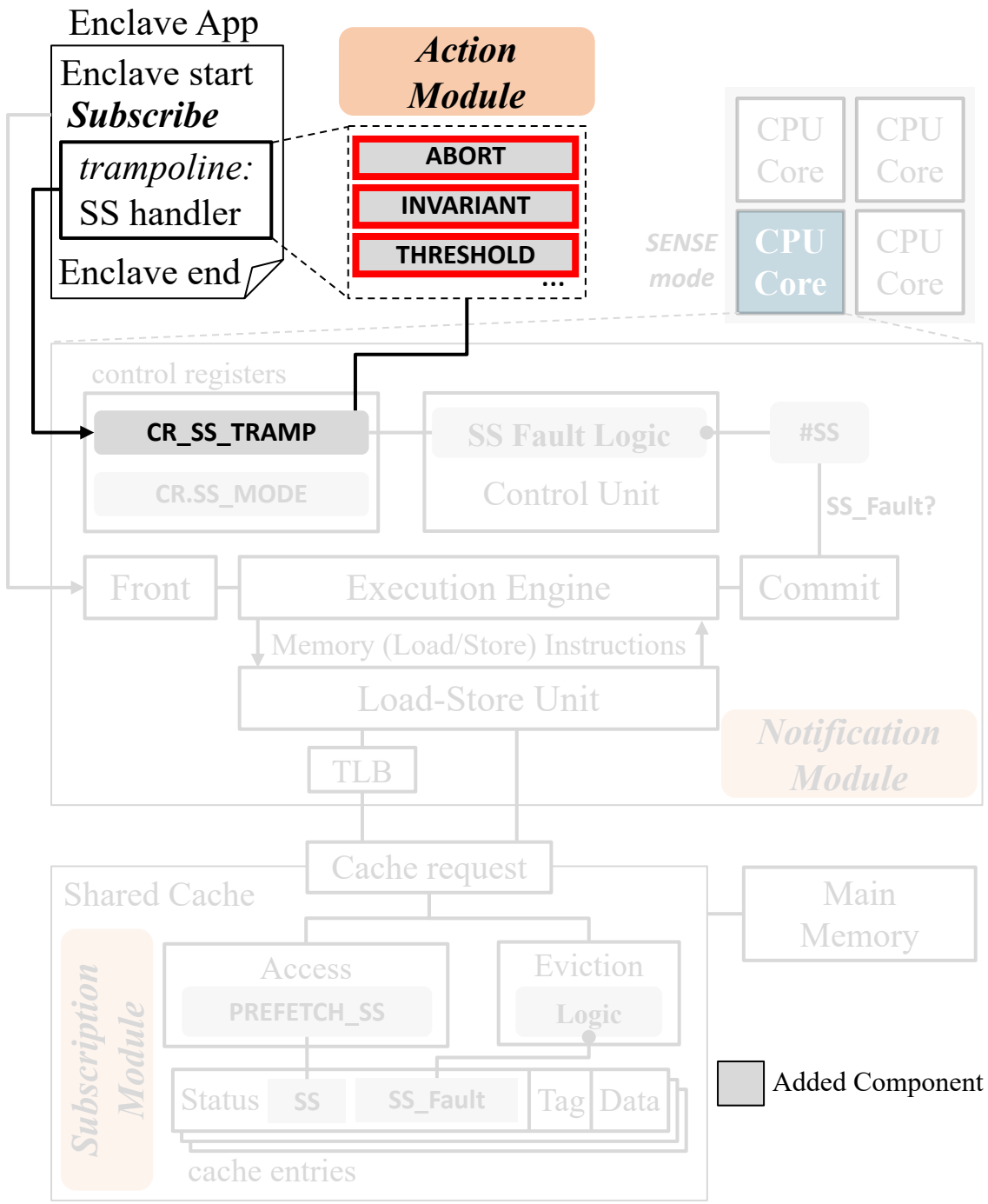
Notification Module

- SENSE control registers
- New ISA instructions
- SENSE hardware fault
- SENSE fault control logic to enter the trampoline



Action Module

- ABORT
  - Abort the process
- INVARIANT
  - Preserve a safety property
- THRESHOLD
  - Local counter for event quota
  - A policy when the threshold is exceeded (e.g., terminate)



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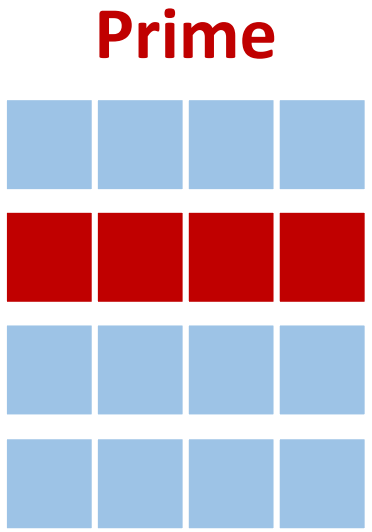

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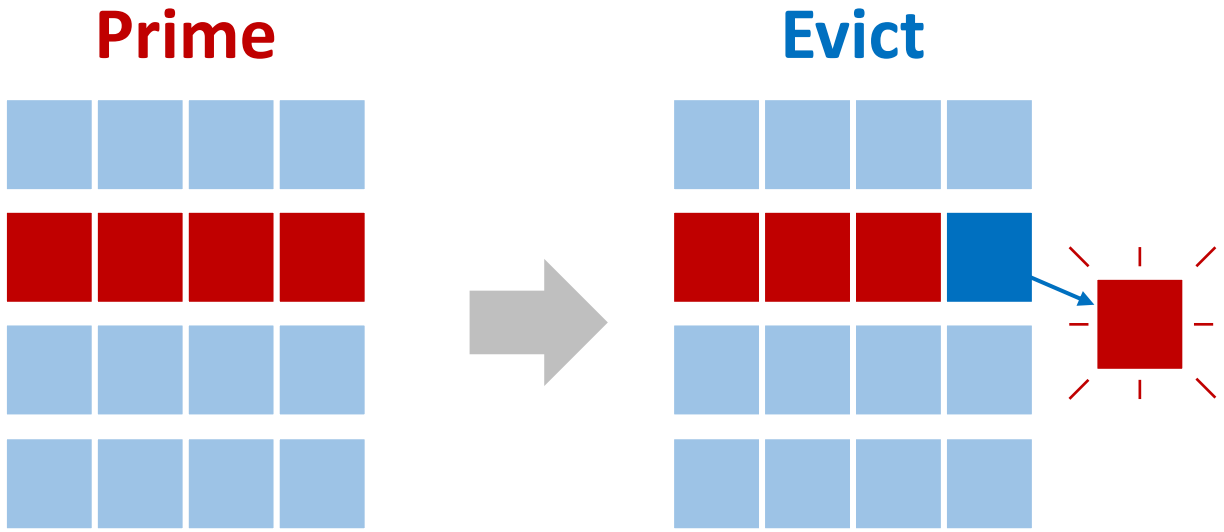

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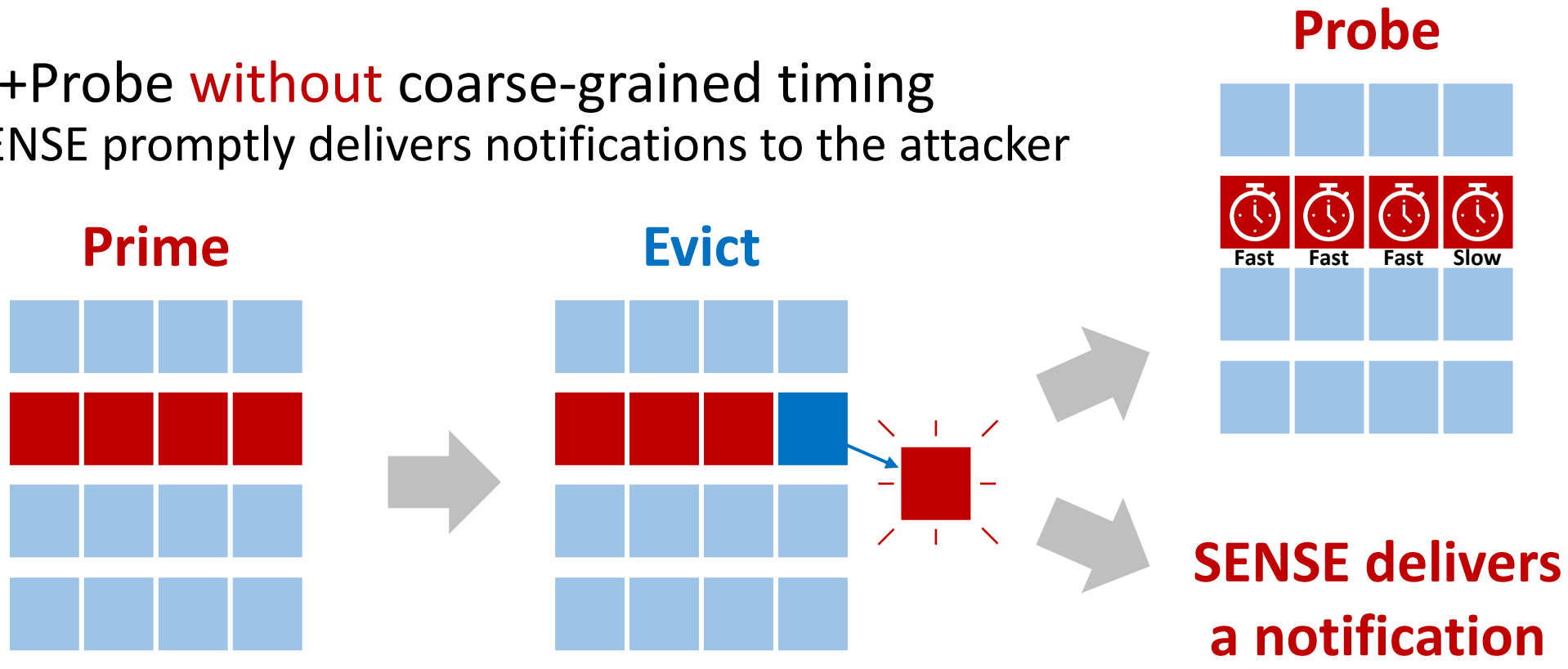

- SENSE does not expose new information to a malicious TEE thread
  - SENSE provides the same eviction information as Prime+Probe, with less noise

Other Use Case: Verifying OS Contracts

- The OS is responsible for management tasks
  - OS-application contract
- Malicious OS does not honor such contracts
- Use SENSE to implement a verification logic
- Example: Cache coloring

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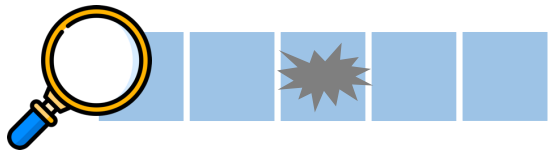

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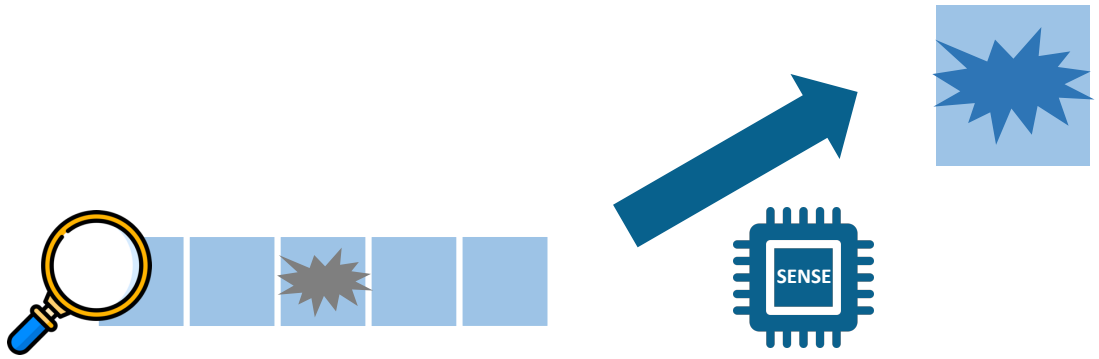

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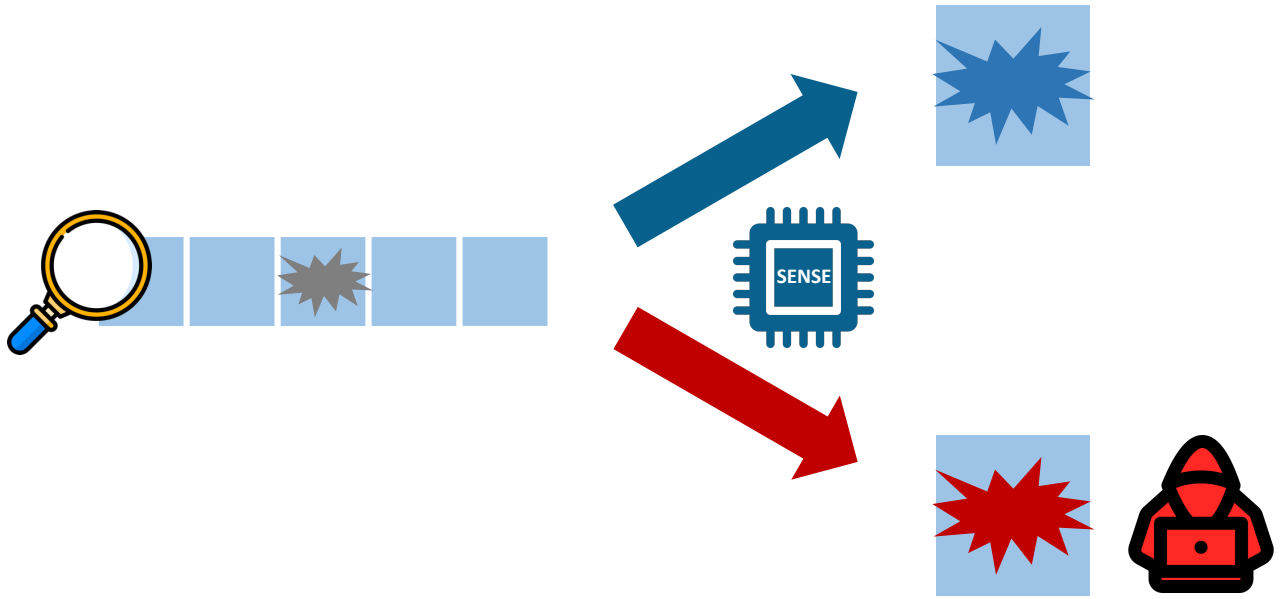

Other Use Case: On-demand Library Loading

- Software-based SCA mitigations have heavy performance overhead
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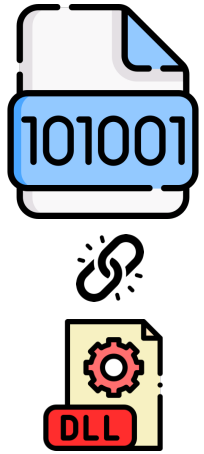
- Ideally, only pay the overhead when necessary
  - Application starts using an optimized library
  - Load the secure version of library if there is a sign of SCAs



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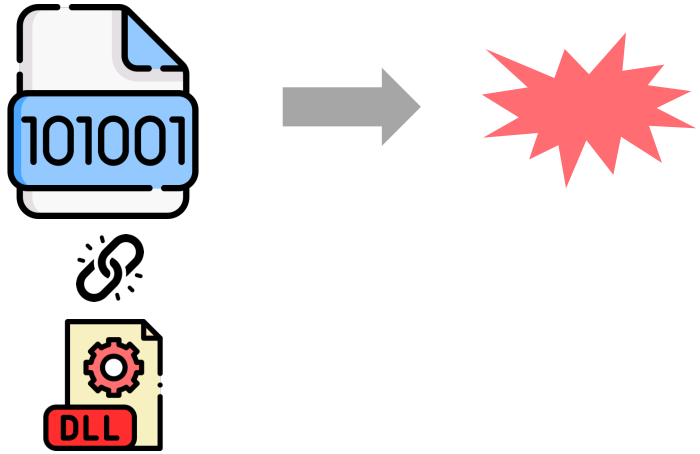

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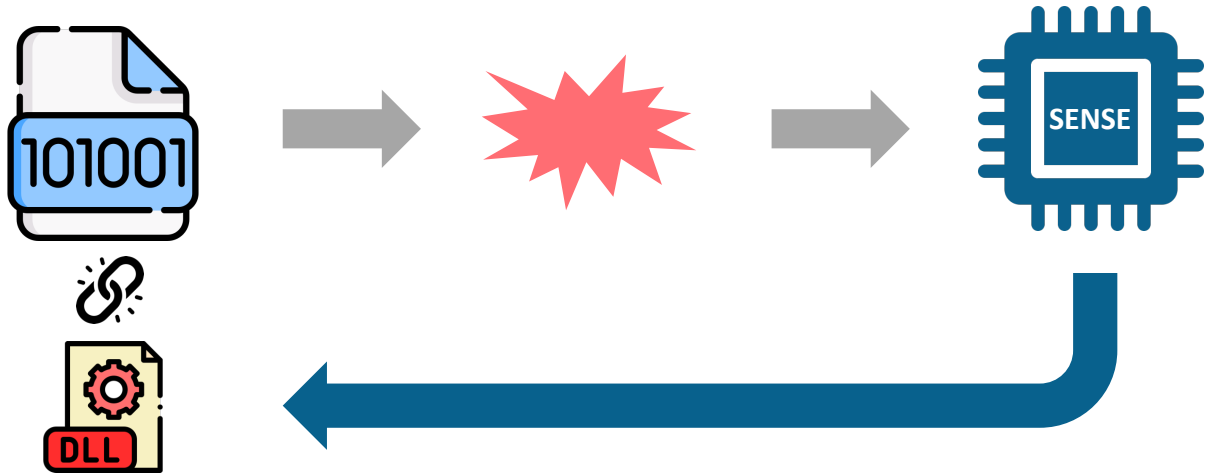

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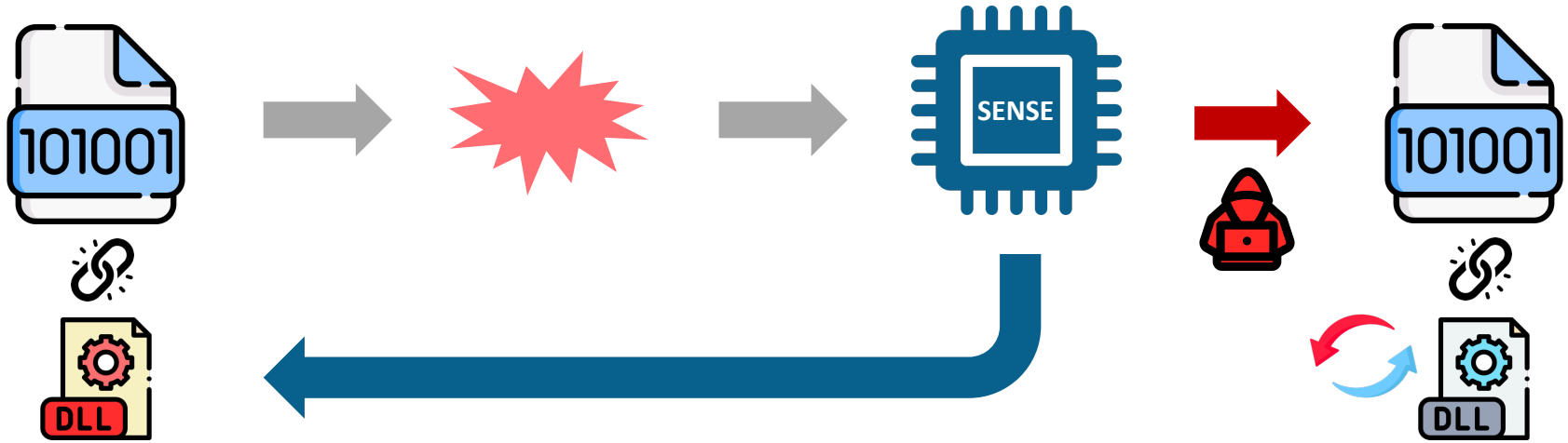

Implementation

- Gem5 simulation
  - CPU SENSE mode
  - CPU micro-code for event notification
  - Enabling SENSE on cache eviction events
- Basic event handlers for cache evictions
  - ABORT (exit(0))
  - INVARIANT (Refetch the evicted cacheline)
  - THRESHOLD (Number of allowed cache. Terminate if exceeded)

Security Evaluation

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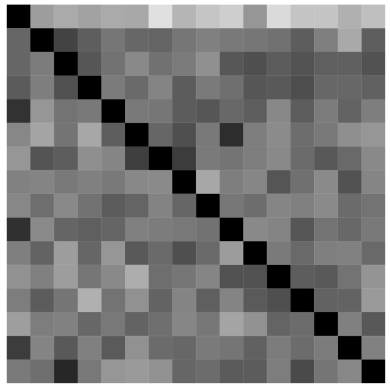

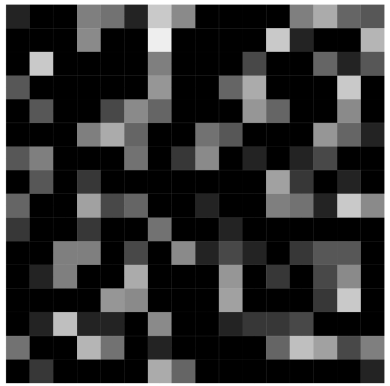

With SENSE + cache INVARIANT handler

Cache hit patterns of the first AES T-Table (Te0) under Prime+Probe attack.

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- Attacker's exploitation of SENSE
  - Probe via SENSE is ~8× faster than probing via timing channel
  - Probe via SENSE has a reduced false positive rate compared to timing channel

  → Efficiency benefits during an actual Prime+Probe attack

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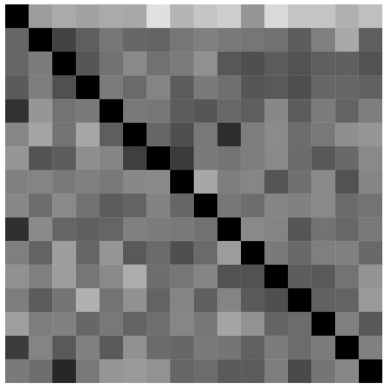

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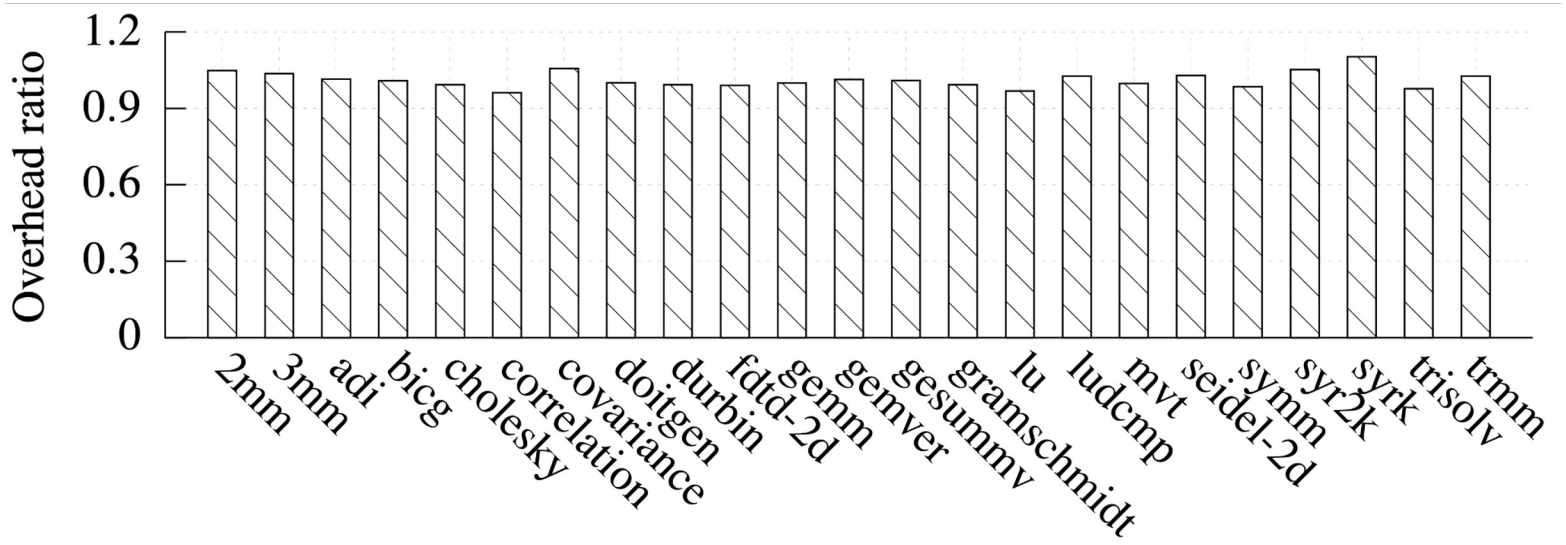
Performance Evaluation

- The performance of SENSE is evaluated on each module:
  - Subscription Module
  - Notification Module
  - Action Module
- PolyBenchC
  - Kernel functions that perform mathematical operations using matrices
  - Kernel functions as critical sections in TEEs monitored by SENSE
  - One matrix is monitored for cache eviction events

Performance Evaluation (Subscription Module)

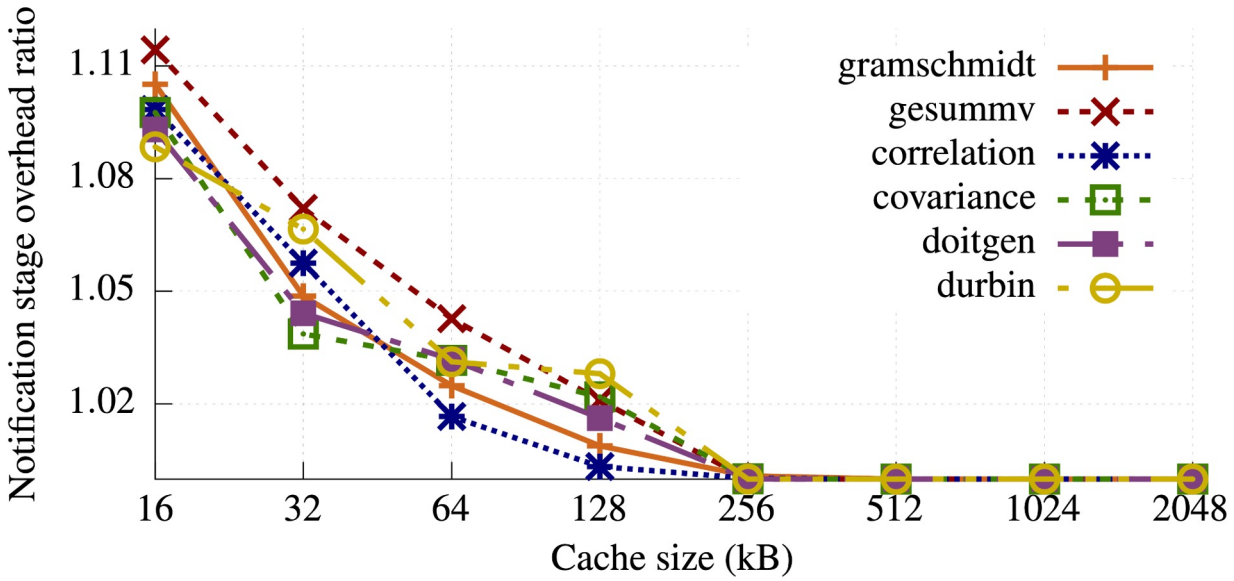
- Initialization: registers trampoline and turns on CPU SENSE mode
- Preparation: prefetching the secret data and mark as monitored
- Average overhead is **1.2%**



Performance overhead of Subscription Module

Performance Evaluation (Notification Module)

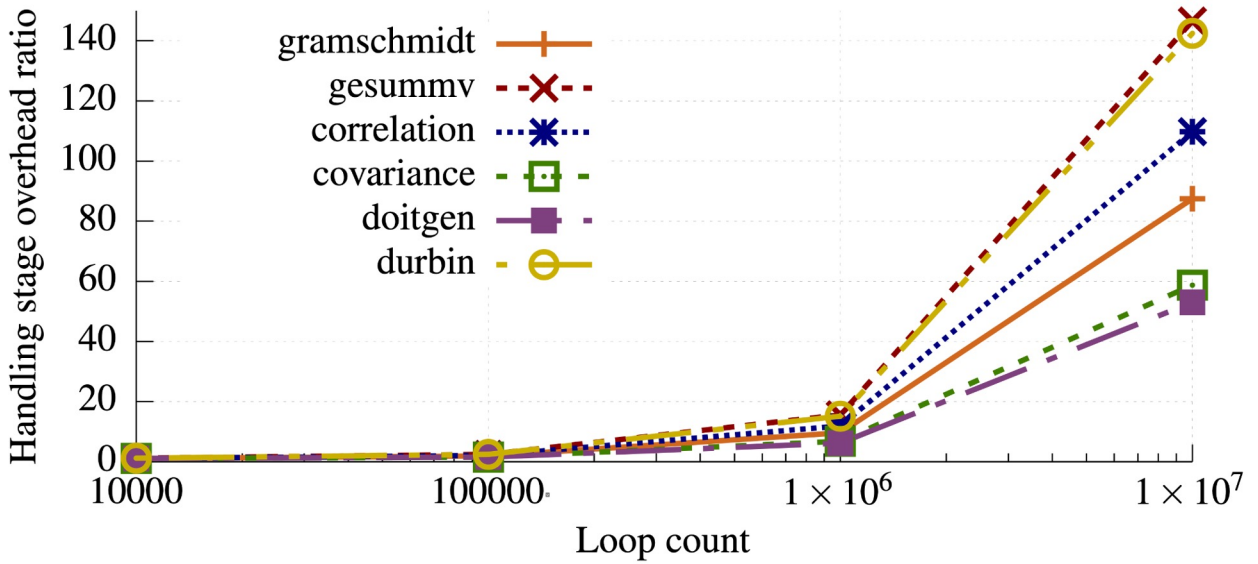
- CPU micro-code for state cleaning and control transfer
- Few events with a large cache size
- Decrease cache size to magnify the behavior



Performance overhead of Notification Module

Performance Evaluation (Action Module)

- Dummy handlers that performs simple operations inside a loop
- Increase the loop variable to simulate the increase of handler complexity
- Cache size of 32 kB (effective to show behaviors)
- Not surprisingly, the performance of the handler dominates



Performance overhead of Action Module

Conclusion

- Addressing **information asymmetry** can allow TEEs to proactively defend themselves against SCAs
- SENSE to turn a side channel exploited by attackers into a direct channel dedicated to users of TEEs
- Performance overhead of 1.2% under benign situations
- Does not degrade security of the TEE

Conclusion

- Addressing **information asymmetry** can allow TEEs to proactively defend themselves against SCAs
- SENSE to turn a side channel exploited by attackers into a direct channel dedicated to users of TEEs
- Performance overhead of 1.2% under benign situations
- Does not degrade security of the TEE

https://github.com/sslab-gatech/Sense

Thank You! (And Q&A)

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