OpenSGX: An Open Platform for SGX Research

Prerit Jain, Soham Desai, **Seongmin Kim***, Ming-Wei Shih, JaeHyuk Lee, Changho Choi, Youjung Shin, Taesoo Kim, Brent Byunghoon Kang, Dongsu Han





- Hardware technologies for trusted computing
 - Isolated execution: integrity of code, confidentiality
 - To protect application from untrusted platform

AMD, ARM Partner on Future TrustZone Security Platform

BY DAMON POETER JUNE 13, 2012 05:15PM EST - 1 COMMENT

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Intel alters design of 'Skylake' processors to enhance security

October 3rd, 2015 at 12:04 pm - Author Anton Shilov

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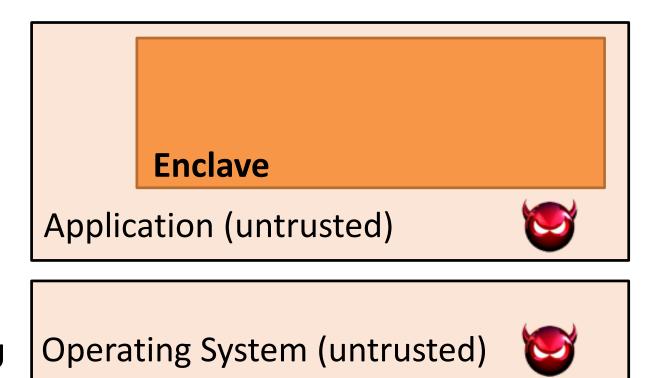
Intel alters design of 'Skylake' processors to enhance security

October 3rd, 2015 at 12:04 pm - Author Anton Shilov

- Practical limitations of TEEs
 - Trusted Platform Module (TPM) : Poor performance
 - ARM TrustZone : Compatibility (only for embedded devices)

Intel SGX

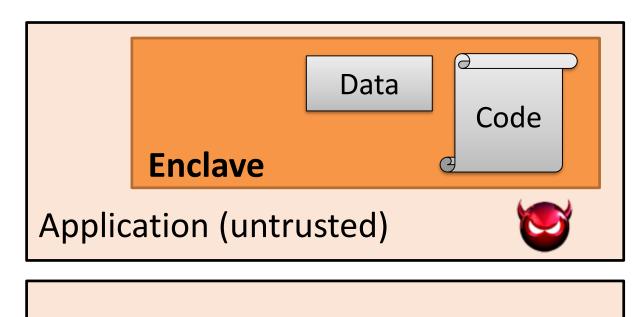
- An extension of x86 Instruction Set Architecture (ISA)
 - Offers native performance, Compatibility with x86
 - Application keeps its data/code inside the "enclave"



Skylake CPU

Intel SGX

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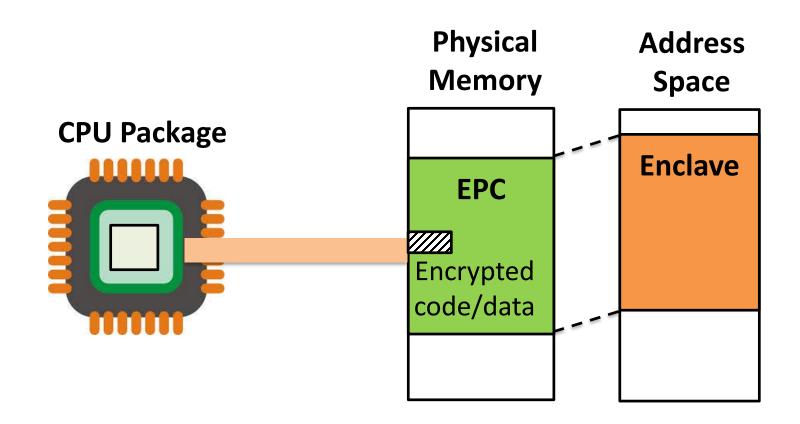


Skylake CPU

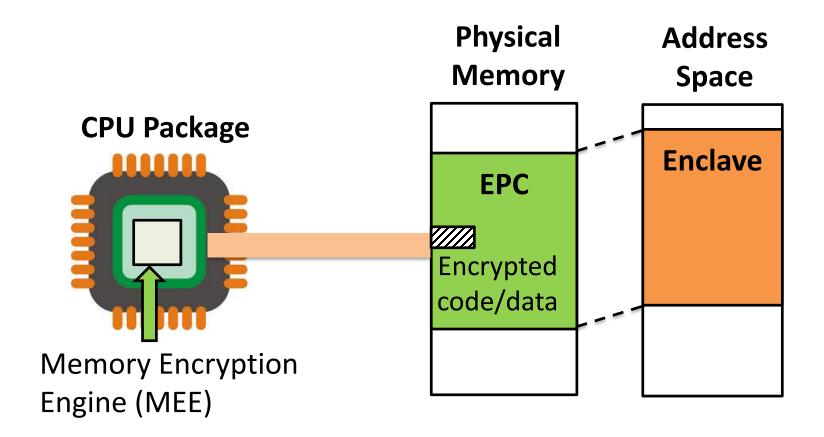
Operating System (untrusted)



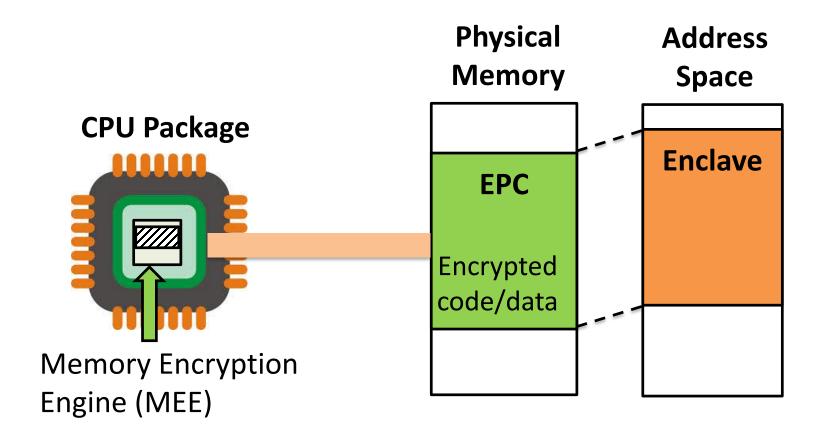
- Smallest attack surface by reducing TCB (App + processor)
- Protect app's secret from untrusted privilege software



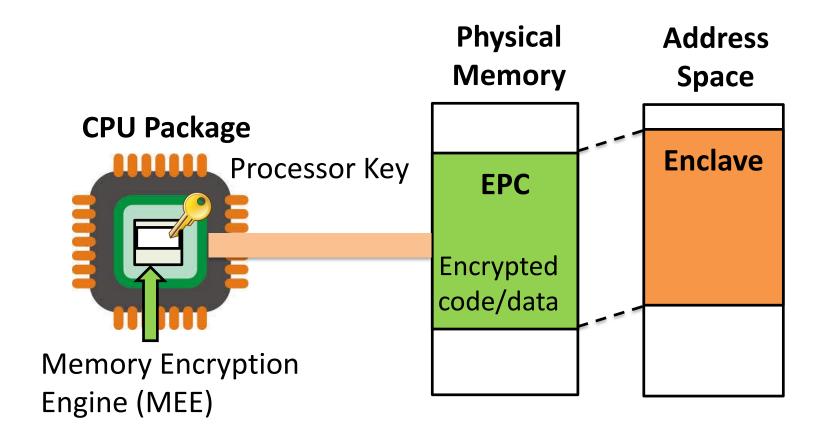
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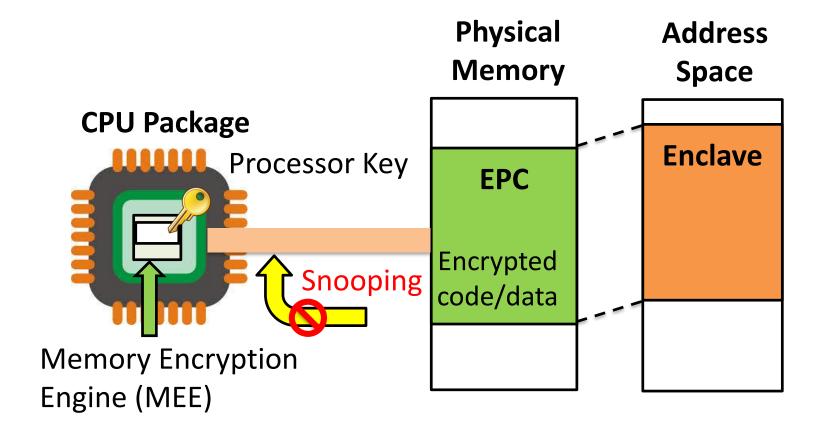
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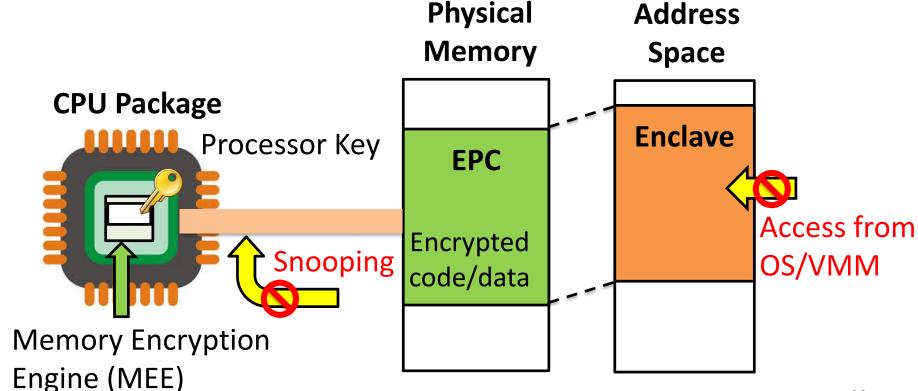
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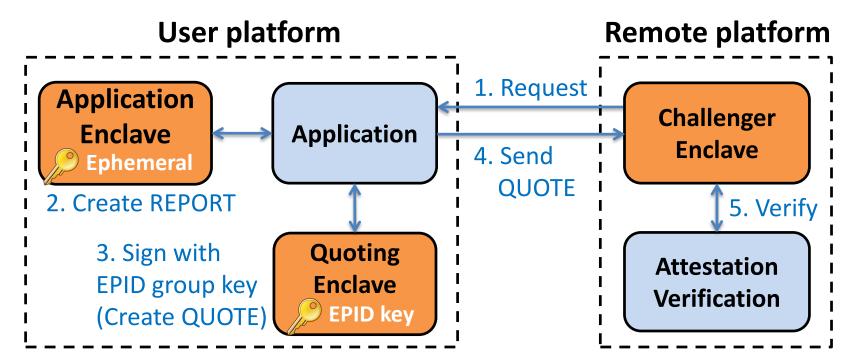


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Intel SGX 101: Remote attestation

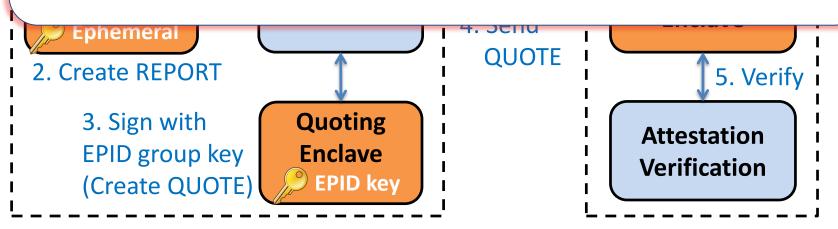
- Attest an application on remote platform
 - Check the integrity of enclave (hash of code/data pages)
 - Verify whether enclave is running on real SGX CPU
 - Can establish a "secure channel" between enclaves



Intel SGX 101: Remote attestation

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Intel SGX brings new opportunities for enhancing security of applications



SGX Research: Current Status

 Pioneering research: Adopting SGX on cloud computing (Haven [OSDI14], VC3 [S&P15])

 Confidentiality verification of SGX program (Moat [CCS15])

Adopts SGX on networking [HotNets15]

SGX Research: Current Status

 However, software technologies for SGX lag behind their hardware counterpart

SGX CPU and SDK is now available! But...

- Specification for SGX [revision 1 & 2] is not fully available on the SGX hardware (only functionalities in revision 1)
- SGX technology has a complex license model

OpenSGX: Design Goal

- Offers a complete platform for SGX research
 - To explore software and hardware design space of SGX
 - To develop and evaluate SGX-enabled applications

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 - To develop and evaluate SGX-enabled applications
- Fills non-trivial issues on SGX software components
 - Support for system software and user-level APIs
 - Familiar programming model and interface
 - Secure design to defend against potential attack vectors (e.g., lago attacks)

OpenSGX: Design Goal

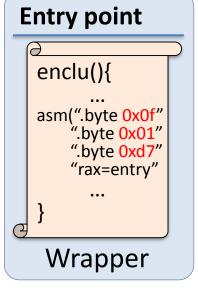
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 - Secure design to defend against potential attack vectors (e.g., lago attacks)
- Non goal : security guarantee

OpenSGX: Approach

- Using userspace emulation of QEMU
 - Binary translation to support SGX instructions
 - QEMU helper routine to implement complex instructions

Host (single address space)

Code EPC Lib EPC ... Data EPC ... Stack EPC Heap EPC Enclave



Binary Translation



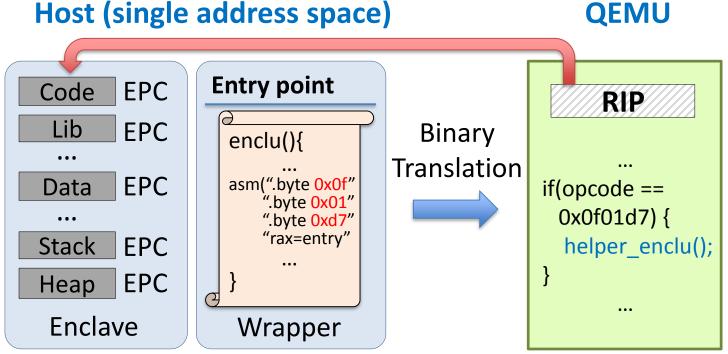
QEMU

Helper routine

- Set registers
- OperatesSGX instructions

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QEMU

Helper routine

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Emulated SGX hardware

- Emulated SGX hardware
- OS emulation layer

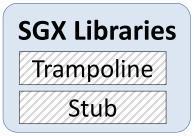
SGX OS Emulation

- Emulated SGX hardware
- OS emulation layer
- OpenSGX user library

SGX Libraries
Trampoline
Stub

SGX OS Emulation

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OpenSGX toolchain

SGX OS Emulation

Emulated SGX hardware

Enclave loader

- OS emulation layer
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Enclave loader Runtime library Stub

SGX Libraries
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SGX OS Emulation

OpenSGX toolchain

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- Enclave loader
- Performance monitor
- Enclave debugger

Enclave loader

Runtime library

SGX Libraries
Trampoline
Debugger

Performance
Monitor

SGX QEMU (HW emulation)

- Emulated SGX hardware
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Enclave Program

Enclave loader

Runtime library

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OpenSGX toolchain

SGX OS Emulation

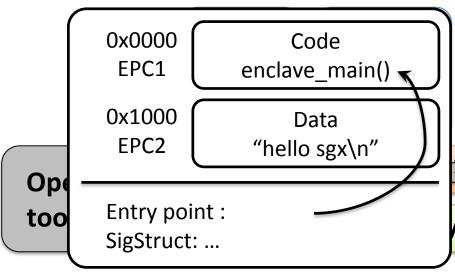
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Enclave Program

```
void enclave_main(){
  char *hello = "hello sgx!\n";
  sgx_enclave_wriate(hello, strlen(hello));
  sgx_exit(NULL);
}
```

\$ opensgx hello.sgx hello.conf hello sgx!



- Emulated SGX hardware 🗸
- OS emulation layer 🗸
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SigStruct: ...

OpenSGX toolchain

Enclave loader

hello sgx!

- Performance monitor
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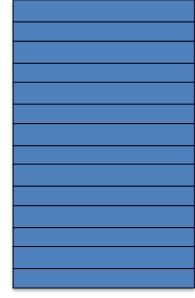
Enclave Program

0x0000 Code EPC1 enclave_main() 0x1000 Data EPC2 "hello sgx\n" Op Entry point: tool

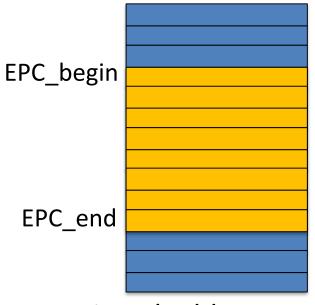
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- Emulates all data structures(e.g., EPCM) and processor key
- EPC Memory management
 - Direct mapping on virtual memory
 - Access protection: Instrument memory access

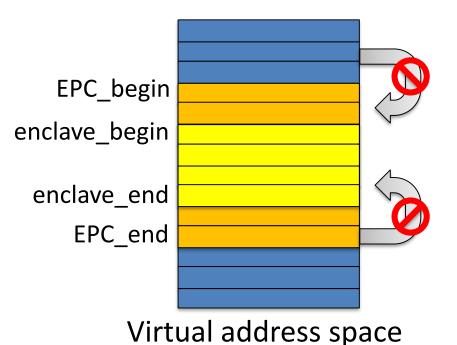
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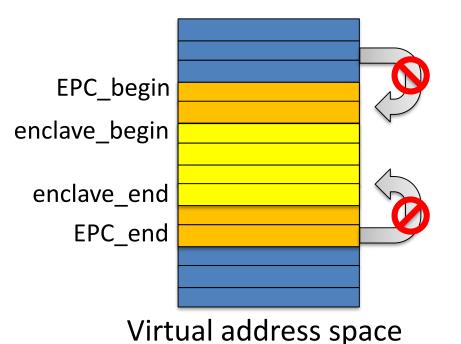
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- 1. Prohibit access from host to EPC
- 2. Prohibit others enclaves' EPC to current enclave's EPC

Hardware Emulation

- Emulates all data structures(e.g., EPCM) and processor key
- EPC Memory management
 - Direct mapping on virtual memory
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```
...
Case (Load | Store) {

1. Prohibit access
from host to EPC
2. Prohibit others enclaves'
EPC to current enclave's EPC
}
...
```

QEMU's translation routine 37

Instruction Support

- OpenSGX supports most instructions specified
 - 21 out of 24 instructions
 - Except for debugging related instructions (e.g., EDBGRD)
 - Instead, it offers rich environment for debugging since it is a "software emulator" (e.g., GDB stub)

Instruction Support

- OpenSGX supports most instructions specified
 - 21 out of 24 instructions
 - Except for debugging related instructions (e.g., EDBGRD)
 - Instead, it offers rich environment for debugging since it is a "software emulator" (e.g., GDB stub)
- Provides simple C APIs which wraps assembly code
 - User-level instructions (ENCLU): accessible to user-level APIs
 - Super-level instructions (ENCLS): Requires system support

OS Emulation Layer

- Emulate OS to execute the privileged SGX instructions
 - Bootstrapping (EPC allocation)
 - Enclave initialization & page translation
 - Dynamic EPC page allocation

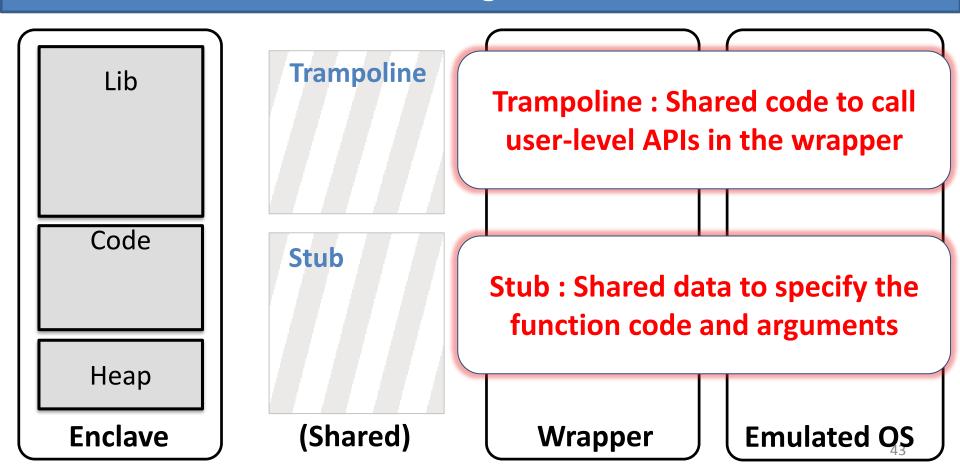
System call	Description
sys_sgx_init()	Allocate EPC memory region
sys_init_enclave()	Create an enclave, Add and measure EPC pages
sys_add_epc()	Allocates a new EPC page to the running enclave
sys_stat_enclave()	Obtains the enclave statistics

OS Emulation Layer

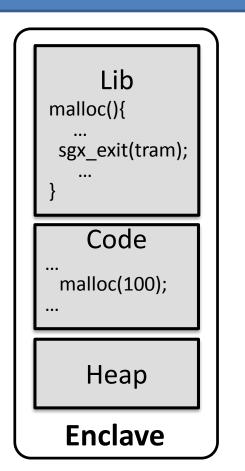
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Planning to extend the emulated OS for the system-level layer

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sys_add_epc()	Allocates a new EPC page to the running enclave
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"A strict and narrow interface to handle enclave-host communication using shared data/code"



Trampoline

```
if (fcode ==
   FUNC_MALLOC)
   alloc_tramp();
...
```

Trampoline: Shared code to call user-level APIs in the wrapper

Stub

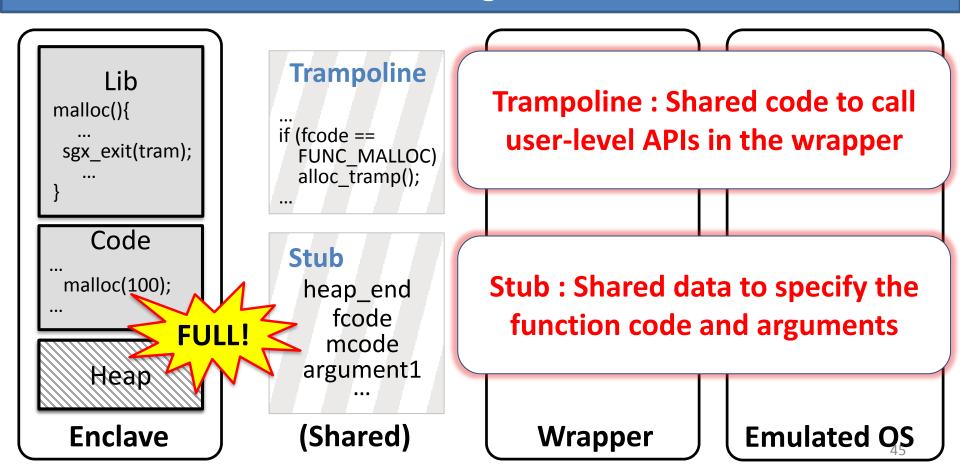
heap_end fcode mcode argument1

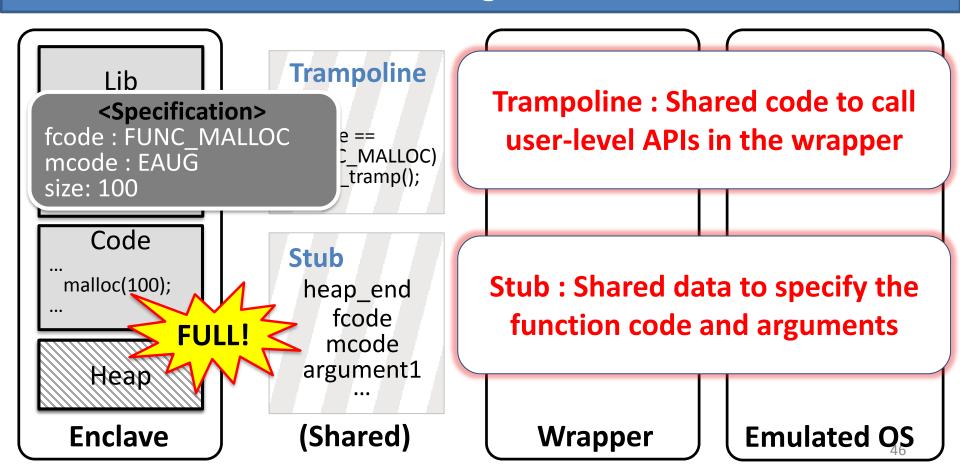
(Shared)

Stub: Shared data to specify the function code and arguments

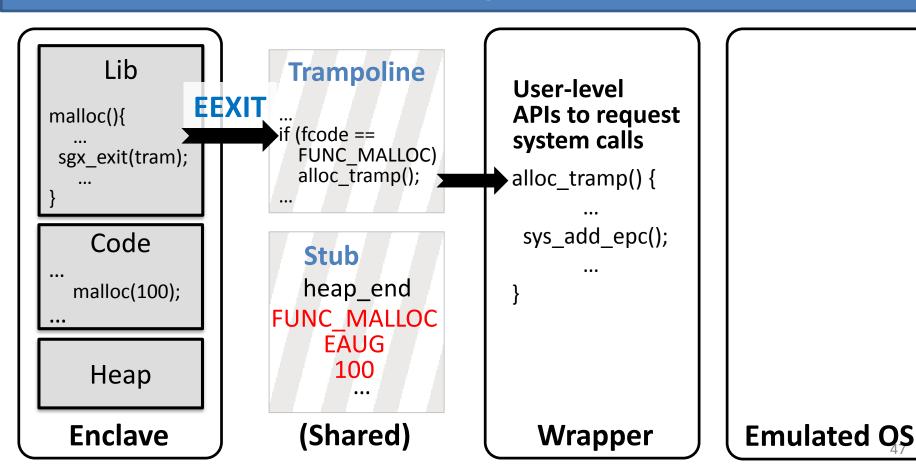
Wrapper

Emulated QS

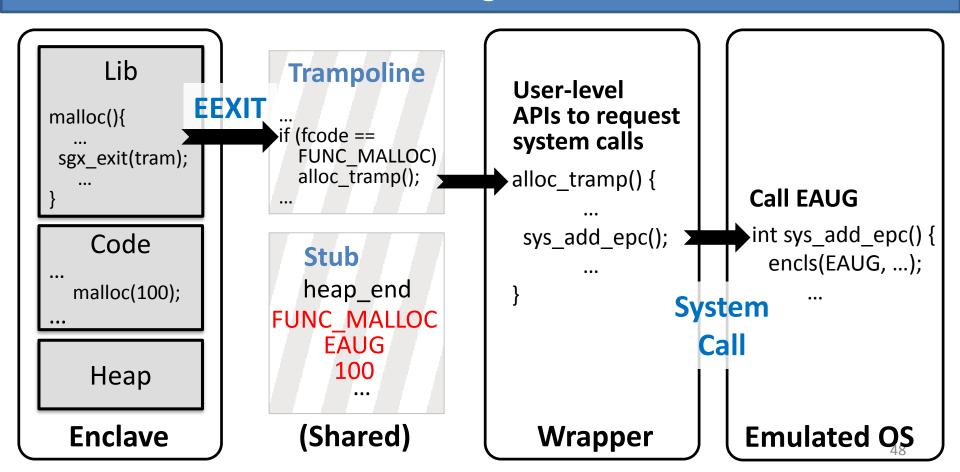




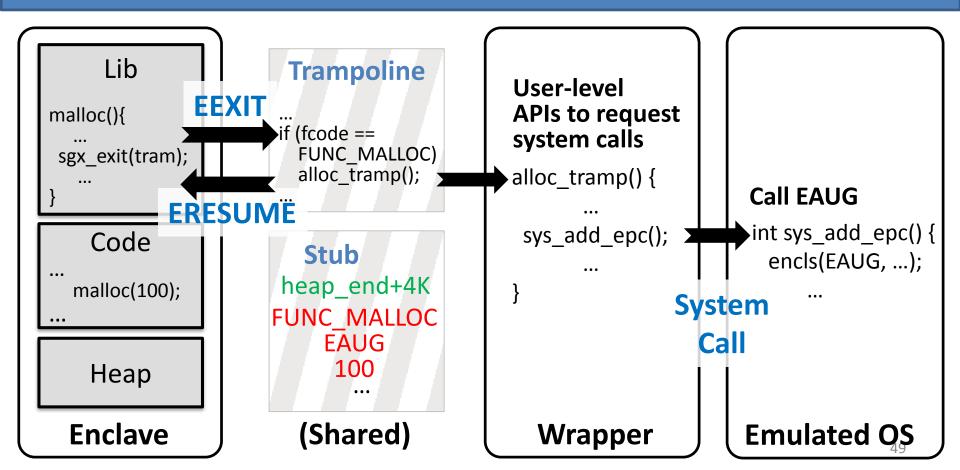
Trampoline and Stub Interface



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Evaluation: Tor Network

- Redesigns non-trivial application to use OpenSGX
- Tor: volunteer-based anonymity network

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"Defend possible attacks on Tor components when they are compromised by adversaries"

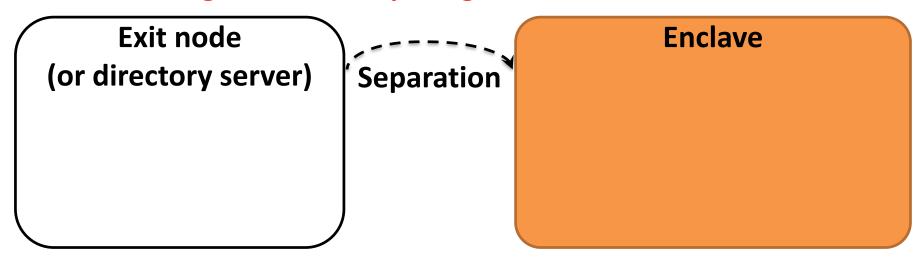
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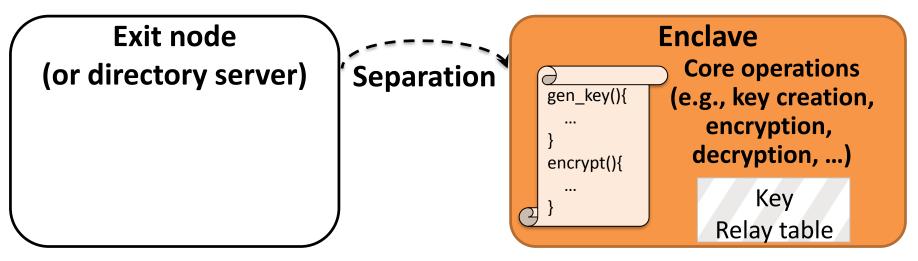
"Defend possible attacks on Tor components when they are compromised by adversaries"

 Here, defense against network-level attacks on Tor is out of scope

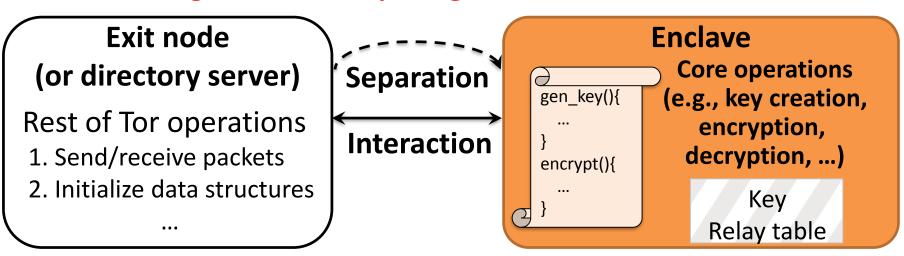
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 - Protect data/code from adversary
 - Reducing Trusted Computing Base



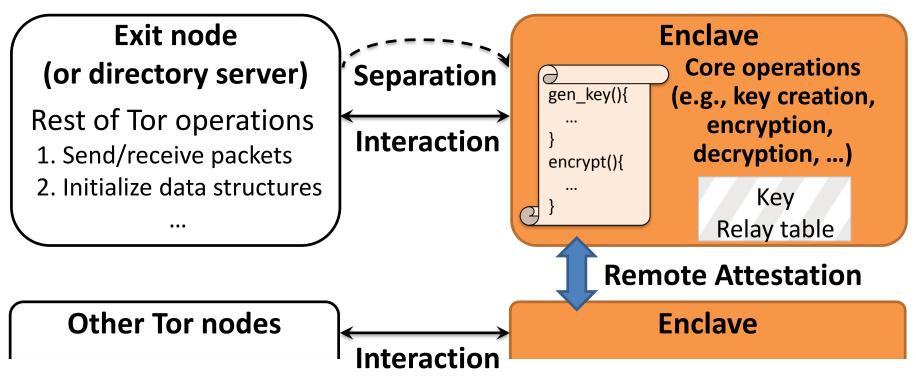
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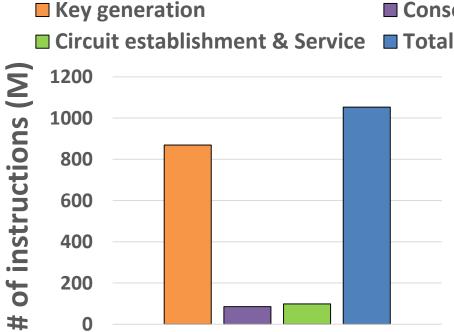


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Performance Profiling

- Performance profiling of Tor exit node
 - Using OpenSGX performance monitor



Consensus creation

(Unit: Number of pages)

	Code	Data	Total
OpenSSL	271	89	360
SgxLib	3	1	4
Tor	4	1	5
Total	278	91	369

Required EPC: Less than 2MB

OpenSGX: Current Status

- Available at github, released in May 2015
 - Available in https://github.com/sslab-gatech/opensgx
 - 7 Contributors (Gatech, KAIST, Two sigma, MITRC, ...)
 - 31 unique cloners, 1,645 Views (Until January, 2016)
- What's next?
 - Binary compatibility with Intel SGX hardware
 - Implement unsupported functionalities (e.g., multi-threading)
- Our current community





Our Early Lessons on SGX

Misconceptions on SGX

- SGX for desktop-like environment : Needs secure I/O channel (integration with hardware technology such as Intel IPT)
- Need EPID support for the remote attestation

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Malicious use of Intel SGX

- Malware might be possible by abusing the isolation property
- Fails on traditional signature-based AV programs

Conclusion

 We design and implement OpenSGX, fully functional and instruction-compatible SGX emulator

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- As a showcasing application, we develop SGX-enabled
 Tor to enhance the security and privacy
- OpenSGX offers opportunities to explore all components of SGX research
 - Hardware semantics (e.g., encryption scheme of MEE)
 - System software, enclave loader and user-level APIs
 - Redesigning unforeseen security applications (e.g., Tor)

Thanks! Any Questions?



SGX Threat Model

"An adversary has control over all software components (including OS and hypervisor) and hardware except the CPU package"

Protection against denial-of-service is out of scope

Comparison: Intel SGX vs OpenSGX

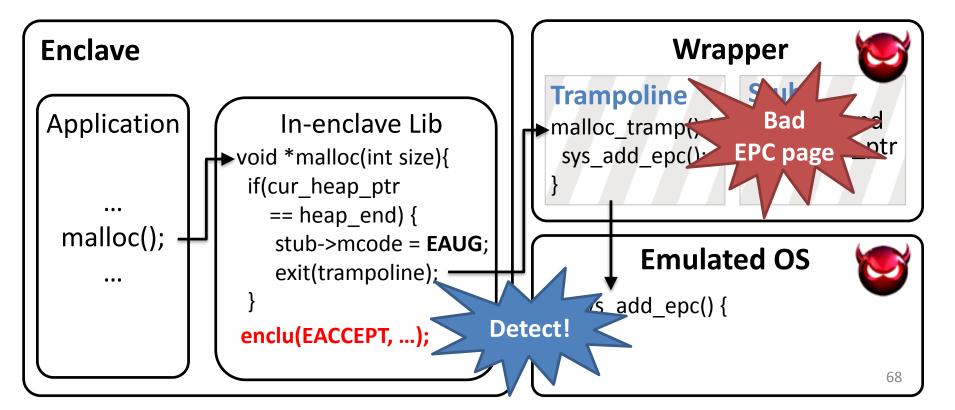
	Intel SGX	OpenSGX
Туре	Hardware	Software Emulator
Instructions	16 ENCLS, 8 ENCLU	13 ENCLS, 8 ENCLU (Except debugging)
Data structures	Specified	0
Paging	Page table	Direct mapping
System software	Not specified	User level emulation
User level APIs	SDK is available (Only for Windows)	0

OpenSGX User Library

- Challenge 1: Facilitate the enclave programming
 - Custom in-enclave library : APIs for user-level SGX instructions
 - Porting standard C library (glibc)
- Challenge 2: Minimize attack surface between enclave and the potentially malicious host process
 - Function call relies on OS features will break an execution of enclave programs
 - Such functions open up new attack surfaces (e.g., lago attacks)

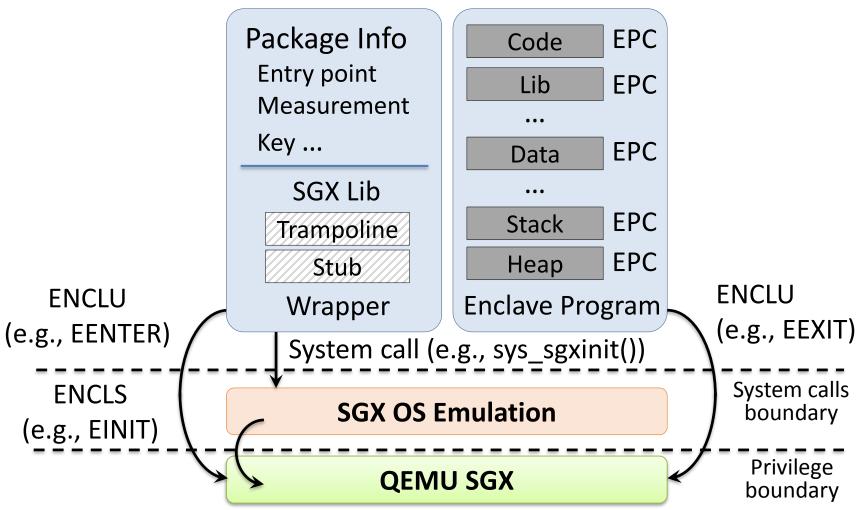
Defense against lago attacks

 lago attacks [ASPLOS'13]: Malicious OS tries to subvert trusted application by incorrect behavior ex) adds incorrect EPC page for heap



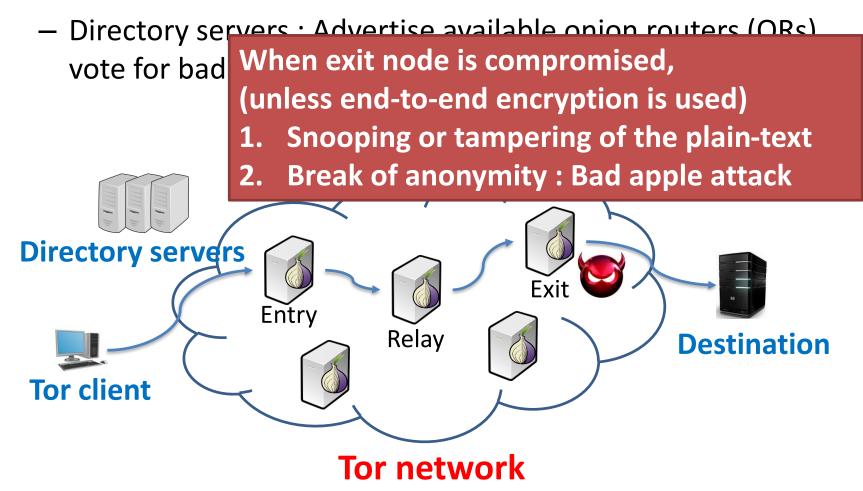
Memory State of OpenSGX Program

User process (single address space)



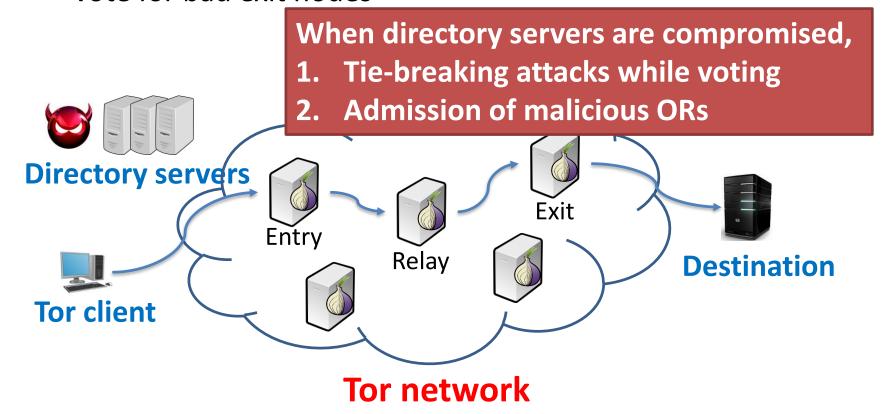
Attacks on Tor Components

Tor network : uses 3-hop onion routing



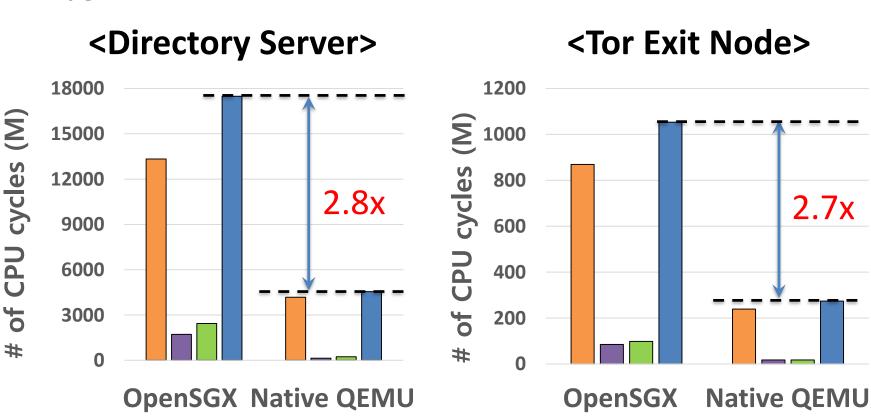
Attacks on Tor Components

- Tor network : uses 3-hop onion routing
 - Directory servers : Advertise available onion routers (ORs),
 vote for bad exit nodes



Performance Profiling: CPU cycles





- ENCLU(EEXIT, ERESUME) calls
- In-enclave library code to handle stub & trampoline interface

Performance Profiling: TCB

<Directory Server>

<Tor Exit Node>

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(Unit: Number of pages)

- Required EPC size: Less than 2MB for each process
- TCB size: 54% smaller than compared to Tor code base

OpenSGX implementation

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 - Modified lines of code: 19K
 - First released in May, 2015
 - 7 Contributors (Gatech, KAIST)
 - 31 unique cloners, 1,645 Views (Until January, 2016)
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